



E-SCIENCE SPACE
NATIONAL UNIVERSITY «YURI KONDRATYUK POLTAVA
POLYTECHNIC»

MONOGRAPH

DATA ERROR CORRECTION
METHOD FOR INCREASING
THE INFORMATION
PROTECTION OF AN
AUTOMATED ROBOTIC
PLATFORM

Warsaw 2024

ALINA YANKO
OLEKSANDR LAKTIONOV
NAZAR PEDCHENKO
STANISLAV BILKO

DATA ERROR CORRECTION METHOD FOR INCREASING THE INFORMATION PROTECTION OF AN AUTOMATED ROBOTIC PLAT- FORM

2024
NATIONAL UNIVERSITY «YURI KONDRATYUK POLTAVA POLYTECHNIC»

Alina Yanko, Oleksandr Laktionov, Nazar Pedchenko, Stanislav Bilko

DATA ERROR CORRECTION METHOD FOR INCREASING THE INFORMATION PROTECTION OF AN AUTOMATED ROBOTIC PLATFORM

Monograph
WARSZAWA 2024

UDC 681.5.09 (004.056.2/.5)

State No. registration number 00124U000621

Authors:

Alina Yanko – PhD in Technical, Associate Professor, Department of Computer and Information Technologies and Systems, National University «Yuri Kondratyuk Poltava Polytechnic», Ukraine. ORCID 0000-0003-2876-9316

Oleksandr Laktionov – PhD in Technical, Associate Professor, Department of automation, electronics and telecommunications, National University «Yuri Kondratyuk Poltava Polytechnic», Ukraine. ORCID 0000-0002-5230-524X

Nazar Pedchenko – PhD in Technical, Senior Lecturer, Department of Oil and Gas Engineering and Technology, National University «Yuri Kondratyuk Poltava Polytechnic», Ukraine. ORCID: 0000-0002-0018-4482

Stanislav Bilko – PhD in Economics, Department of Finance, Banking and Taxation, National University «Yuri Kondratyuk Poltava Polytechnic», Ukraine. ORCID: 0000-0003-0259-4482

Data error correction method for increasing the information protection of an automated robotic platform. A monograph /Yanko A., Laktionov O., Pedchenko, N., & Bilko, S. – E-SCIECE SPACE, WARSZAWA, 2024 – 62 p.

ISBN 978-83-961636-5-3

DOI 10.54658/ESS.monograph.2024.pp.1-62

The monograph was prepared as part of the young scientists research work (registration number 00124U000621) with the financial support of the Ministry of Education and Science of Ukraine. All rights reserved. No part of this book may be reprinted or reproduced or utilized in any form or by any electronic, mechanical, or other means, now known or hereafter invented, including photocopying and recording, or in any information storage or retrieval system, without permission in writing from the authors.

CONTENTS

INTRODUCTION	4
CHAPTER 1. THEORETICAL FOUNDATIONS OF INFORMATION PROCESSING SYSTEMS AND THE PROCESS OF ERROR CORRECTION IN AUTOMATED ROBOTIC PLATFORMS	10
CHAPTER 2. JUSTIFICATION OF THE IMPORTANCE TO CREATE INFORMATION PROCESSING SYSTEMS BASED ON THE USE OF A SYSTEM OF RESIDUAL CLASSES	15
CHAPTER 3. FORMULATION OF PRINCIPLES FOR CONTROL OF NON-POSITIONAL CODE STRUCTURES IN THE SRC	19
CHAPTER 4. RESEARCH OF CORRECTIVE POSSIBILITIES OF CODES IN THE SRC	24
CHAPTER 5. DEVELOPMENT OF A METHOD FOR DETECTING AND CORRECTING ERRORS IN THE SRC BASED ON THE USE OF <i>L</i> -CODES	37
CONCLUSION	53
REFERENCES	57

INTRODUCTION

The current stage of information society development is characterized by the active development and implementation of progressive information technologies based on the widespread use of various data processing systems. The increase in volumes of information circulating in the digital space requires the use of highly efficient data processing systems that must function in real time with minimal time costs. That is, the scale and complexity of the tasks solved by modern information and computer means present qualitatively new requirements to its. This determines the need to improve existing and create new means of information processing [1].

At the same time, the efficiency of information data processing must be accompanied by ensuring its security. The issue of data security becomes especially relevant in the context of increased information and cyber terrorism. Information security is an integral component of every sphere of national security and is designed to protect the vital interests of the individual, society and the state [2]. Ensuring information security becomes a critically important goal in the aspect of strengthening the national security of the state. In this monograph, the main emphasis will be placed on the issue of data correction (control, data diagnostics, detection and correction of errors) in the process of information processing in order to increase the level of its security.

In connection with the complication of scientific and technical tasks of processing ever-growing arrays of information, the trend in the development of information technologies and systems is aimed at increasing the speed (productivity) and reliability of the implementation of the data processing process by modern information processing systems (IPS). After all, the growing complexity and volume of computational tasks require a significant increase in the speed and reliability of arithmetic operations, since all tasks in the IPS consist of a large set of elementary operations: addition, subtraction, multiplication, etc. External and internal negative influences affecting the information processing process in the IPS distort the information, which leads to errors in the calculation. In this case, the bandwidth of existing communication channels cannot always ensure high-quality processing of information in real time.

Digitization processes in the military sphere, which involves the use of various information processing systems (signals, images, navigation coordinates, etc.), require highly accurate and reliable processing of a continuous flow of data in real time. Modern IPS provide an opportunity to digitize all types of information and automate this process, store data, process and distribute processed information, as well as continuously monitor the state of the state's defense capability systems in real time. However, the issue of increasing the reliability of the IPS and data security against unauthorized influences and access remains extremely relevant and unresolved. Because the transformation into a new digital space is not only a tool for realizing national security interests, which creates new opportunities for strengthening the state's defense capabilities, but also a source of new risks and threats to national security in all its components. In the conditions of the development of information technologies (cyber technologies), which is characterized, on the one hand, by the intensification of modern information technologies in all fields, and on the other hand, by an increase in the scale and frequency of cyber-attacks, the emergence of new risks and

security, creating completely new dimensions for conducting information warfare, which affects all sectors of life in the country [3].

The armed aggression of the Russian Federation against Ukraine exacerbated the military challenges and threats posed not only to domestic defense systems, but to all European countries and beyond. In the conditions of war, the country needs a restructuring of strategic goals with a change in the priority areas of the security concept. After all, any hostilities are accompanied not only by military invasion, but also by cyber warfare, and it is precisely in this that an important component of victory is found. In Ukraine, in times of war, it is important to oppose the enemy not only on the battlefield, but also in the information space.

Currently, there are many variations of intrusion detection and prevention systems of various complexity and structure, which are organized by hardware, software, and/or software-hardware. At the same time, the level of cybercrimes related to unauthorized access to information resources grows exponentially every year. The level of protection of Ukraine against digital threats according to the international rating of The Network Readiness Index is significantly lower than in European countries, which indicates a threat to the beneficial development of digitalization and the generation of cross-border threats to EU countries [1]. Today, the protection of each individual element loses its significance, and the problem of creating a complex of reliable protection of the entire information infrastructure of the state as a whole, and especially defense capability systems, arises. Therefore, based on the analysis of scientific developments in the field of cyber protection, it was concluded that there is a need for an effective comprehensive concept of information protection at the data processing stage, through effective monitoring (diagnosis and control) and correction (detection and correction of errors) of data.

Information technologies, an integral element of which are IPS, are rapidly developing and have great potential in many fields, including: national security, defense, military medicine, military logistics, intelligence and counterintelligence, aerial reconnaissance, etc. Moreover, in the conditions of war in the 21st century, the share of military personnel involved in active combat operations is minimized. The use of robotic systems is increasingly observed. The use of robotic systems will make it possible to conduct combat operations in the most unpredictable conditions, reducing the loss of personnel. Units using robotic systems gain advantages in time and space, achieving tactical, operational and, most importantly, strategic superiority over the enemy in combat. Usually, robotic systems are implemented on the basis of the use of advanced information and communication technologies (navigation systems, computer systems, automated control systems, IPS, etc.). Ground robotic complexes and UAVs (especially FPV drones, which are very actively used on the battlefield) require constant processing of a large amount of information, which is mostly added in integer form: navigation data (coordinates, and other data that allow determining the position and speed of movement about object on the Earth's surface or in the atmosphere), continuous monitoring of the topography of the area, etc. Thus, the development of highly reliable IPS systems of defense capability is under the special control of the heads of states and governments and belongs to the category of strategically important and urgent problems of scientific and technical developments, which also confirms the relevance and importance of research conducted in this direction.

In connection with the above, the issue of ensuring the security of automated robotic platforms (ARP), in conditions of war and growing cyber threats, due to the use of the latest circuit solutions resistant to failures and cyber-attacks and the development of effective IPS based on alternative mathematical solutions, is actualized. Since data processing in the IPS involve operations performed on numbers presented in the form of special machine codes in the accepted numeral system. Features of the applied numeral system determine the effectiveness of the IPS functioning as a whole. Therefore, one of the ways to solve the problem is the development of the IPS based on alternative numeral systems. The problem of choosing a numeral system for presenting numbers in the IPS is of great practical importance. In the case of its selection, such requirements as the reliability of the presentation of numbers when using physical elements, economy (the use of such counting systems in which the number of elements for presenting numbers from a certain range would be minimal) are usually taken into account.

One of the most common numeral systems used in most modern computer systems and computer systems in general is the binary system, which refers to the positional numeral system (PNS). There are two main principles of increasing the reliability of the IPS that function in the PNS: increasing the reliability of individual logical elements and circuits (using a new element base) and introducing different types of redundancy (using different types of reservation that affect the reliability of the operation of the IPS). Since the reliability of logic elements is mainly determined by the level of technology development, it is obvious that the introduction of redundancy when using the existing element base is the most effective way to increase the reliability of the operating in the PNS. As a result, one of the effective practical methods of increasing the reliability of the IPS with the use of the PNS is structural reservation, for example, at the level of duplicated or tripled majority structures of information processing. However, the use of structural reservation complicates the structure of the IPS, leads to an increase in energy consumption, mass-dimensional indicators and worsens other important technical characteristics, which ultimately increases the cost of its creation and operation, as well as limits the scope of its application for processing information in various information and control systems and for different conditions of its functioning, which negatively affects the technical characteristics as a whole [4]. The variety of operating conditions of the IPS of robotic complexes and UAVs and the strictness of the requirements (the need to ensure a high degree of calculation accuracy, high productivity and reliability of the operation of the IPS in real time, high speed of information transmission and processing, operational recovery of the operational state of the IPS after failures and failures, etc.), which applied to the modes of operation and operation of the IPS, do not always allow effective application of various types of reservation. Moreover, ARP and UAVs have rather limited mass and size parameters, which are limited, first of all, by the level of energy consumption and maneuverability of these objects.

At the same time, the results of research into the ways of efficient processing of integer data showed that it is impossible to achieve a drastic increase in speed and reliability within the limits of PNS. This is due, first of all, to the presence of inter-bit connections between the processed numbers in the PNS. These connections have a negative effect on the structure of the IPS and methods of implementation of arithmetic operations; limit the speed and reliability of performing arithmetic operations. Also, the presence of inter-bit

connections makes it impossible to parallelize the solving algorithms at the level of elementary operations, as a result of which the performance (speed) of data processing deteriorates. An error that occurred in one binary digit, in the process of transfer from lower to higher digits, spreads over the entire length of the machine word [4]. This circumstance determines the fact that the failure (denial) of the information processing scheme of one binary digit can cause not only single, but also multiple errors in the obtained result. Thus, the unsolved problem of highly productive and highly reliable functioning of the IPS operating in the PNS once again emphasizes the importance of this topic.

The current state and prospects for the development of the IPS of the ARP confirm that the success of its further improvement is impossible without the use of ultra-reliable, high-performance and failure-resistant information processing tools. The above-mentioned shortcomings of existing IPS operating on the basis of PNS necessitate the development and application of fundamentally new methods of increasing the productivity and reliability of the IPS of the ARP, based on the use of new principles and ideas. In particular, information processing methods based on new numeral systems.

Based on the fundamental concepts, provisions and results of number theory, a non-positional system of counting in residual classes was created, the use of which made it possible to obtain interesting results in the field of implementation of arithmetic operations. The system of residual classes (SRC) is a numeral system in which numbers are represented as a set of non-negative residues by a group of mutually prime bases. In connection with this presentation, it became possible to perform rational operations without taking into account the bit relations between the digits of the number. This scientific direction is the development, on the one hand, of the idea of multi-residue AN-encoding of data in PNS and, on the other hand, of cluster data processing systems.

Researches have shown that the use of a non-positional numeral system, namely SRC, as a numeral system of the IPS can significantly positively solve the scientific and practical task of ensuring the reliable operation of the ARP without reducing the productivity of information processing and with a significant reduction, compared to PNS, of the amount of additional necessary equipment. This circumstance makes it possible to significantly increase the reliability of the IPS, as well as to improve some important technical and economic characteristics of the ARP.

However, with the proven fact of the effective use of the SRC in the creation of the IPS of the ARP, the implementation of methods and algorithms for error control and correction is time-consuming or difficult in technical implementation, which reduces the overall effectiveness of the SRC use. This is explained by the fact that the operations of control and correction of information errors in the SRC are non-positional operations, which are the most difficult to implement in this numeral system. It was the unsolved task of simplifying the implementation of control schemes and error correction in the IPS of the ARP operating in the SRC, taking into account the requirements for information processing productivity, on the one hand, and the positive preliminary results of research into the effectiveness of using non-positional code structures, that determined the goal, the scientific and applied task, which is solved in this monograph.

The purpose of the monograph is to increase the simplicity of technical implementation and the efficiency of control and correction of data errors of the IPS based on the

application of corrective properties of L -codes of the SRC, which will ensure the security of the ARP.

To achieve the goal of the monograph, it is necessary to formulate and solve an important and relevant scientific and technical task. The scientific and technical task of the research consists in the development of an effective method of detecting and correcting errors in the SRC based on the use of linear L -codes. The use of the results of solving the main above-mentioned task will contribute to the further development of the theory and practice of non-positional machine arithmetic in the field of control and diagnosis of data presented in the SRC. This, in turn, makes it possible to expand the scope of effective use of the SRC as a numeral system for integer data processing systems.

The first chapter of the monograph examines in detail the theoretical foundations of the principles of operation and purpose of the IPS of the ARP. A review of the literature in this field of science was carried out and the main shortcomings of the existing options for submitting, reading and processing information by automated systems were analyzed. The results of the analysis showed the shortcomings of known IPS operating in the PNS, which actualizes the interest and relevance of research in the direction of finding new numeral systems. The error correction (detection and correction) process in the information code structure of the IPS of the ARP data, which consists of control, diagnosis and correction of errors in the data code structure, is also briefly considered.

In the second chapter, the dependence of the effectiveness of the ARP systems on the IPS is investigated. The main advantages of non-positional counting systems, namely SRC, are listed in detail and constructively, on the basis of which the importance of creating the IPS of the ARP based on the use of the SRC is substantiated.

In the third chapter, with the aim of determining the possibility of creating effective methods, systems and means of operational data control, which is the main stage in the process of error correction in the SRC, the basic principles of control of non-positional code structures in the SRC are formulated. It was concluded that the most rational organization of the control system is the combined control method, which combines hardware and software control methods and meets all the requirements for control systems of the IPS of the ARP.

The fourth chapter examines the corrective properties of non-positional code structures and provides the theoretical basis for correcting data errors in the SRC. The main provisions and conclusions of the theory of failure-resistant data coding in the SRC are presented. On the basis of the provisions of the theory of failure-resistant data coding, research was carried out on the corrective properties and capabilities of the non-positional code structures with different methods of introducing information redundancy, that is, with different numbers and sizes of additional control bases. This made it possible to create a procedure for varying the possible corrective abilities of the failure-resistant code in the SRC during the computational process.

In the fifth chapter, algorithms and a method of error correction based on the use of mutually non-prime bases in the SRC are presented based on the main theoretical principles

of correction of non-positional code structures. It is proved that the use of codes with mutually non-prime bases (*L*-codes) allows expanding the class of errors that are corrected. This significantly expands the corrective capabilities of *L*-codes in the SRC.

The relevance of the development of error control and correction methods is also correlated with priority topics according to the order of the Ministry of Education and Science No. 1104 dated September 7, 2023. (item 5 "Development of the latest remotely controlled systems (complexes) of weapons and military equipment to solve problems related to the insufficient range and immunity of control channels and the insufficient level of automation and autonomy of robotic platforms").

Meaningful and thorough research was made possible with the financial support of the Ministry of Education and Science of Ukraine as part of the implementation of the National Development Program of Young Scientists "Development of an automated robotic platform for demining, reconnaissance and combat missions" (state registration number 0124U000621).

CHAPTER 1. THEORETICAL FOUNDATIONS OF INFORMATION PROCESSING SYSTEMS AND THE PROCESS OF ERROR CORRECTION IN AUTOMATED ROBOTIC PLATFORMS

The basic theoretical and methodological foundations of creating information processing [5], provide for the procedure of developing IPS of the ARP. Information systems support the life cycle of ARP [6], IPS provide automation of robotic processes, mostly in real time [7]. Management of robotic platforms is also carried out autonomously, using IPS tools. At the same time, as stated in the review [8], autonomous IPSs are sensitive to the signal level, and signal loss can affect operation of the ARP. In addition to the loss of the information processing signal, robotic platforms have limitations in battery capacity, weight, and protection against unauthorized access.

According to [9], the IPS of the ARP process can be differentiated into three parts. The first is detection (sensing), conversion and collection of input data signals. The second is data processing and calculation of ARP control actions. The third is the transfer of control data to the working elements of the ARP. The hardware and software and architecture of the IPS used in ARP are limited by significant requirements, namely, power supply, reliability and accuracy of calculations, quick response to commands, complexity of applied applications, etc. [10]. Also, according to the work [11], modern IPS should ensure safety, convenience, stability, speed and quality. The specified requirements should be taken into account when creating new or modernizing existing IPS.

Therefore, IPS is a key element for automating robotic processes, ensuring its efficient functioning. It plays an important role in today's technological field, and its development must be carried out taking into account the requirements of the market, as well as using advanced technologies and approaches. At present, there are many ways and approaches of processing information in the ARP, some of it were considered in the process of reviewing literary sources in this area. In the work [12], IPS with additional intrusion detection capabilities is proposed, where the robotic platform is connected to a local network, which is characterized by a reliable computing infrastructure. The effectiveness of intrusion detection is achieved due to the principle of remote control and machine learning. At the same time, control and correction of errors at the level of arithmetic-logical systems (the numeral system used) is not foreseen.

As can be seen from the works [8, 10], the tools of information processing are characterized by selected calculation systems, and various types of information are supplied to the IPS input. The work [13], in which IPS is proposed for determining the location of radioactive substances, where the output data were recorded by means of Compton cameras and a light range detection and detection camera, is a confirmation of the processing of different information by IPS tools.

In work [14] IPS is used to process network intrusions based on the ROSIDS23 dataset, the data set of which was collected using ROS by means of the tcpdump network protocol analyzer. In addition to network intrusions, IPS is able to process information from navigation systems at a certain speed [15].

The speed of information processing can be diagnosed by a special indicator that measures the time of various procedures from preparatory to transformation of information for management [16]. To accelerate the speed of information processing in the ARP, various methods are used, including pre-processing of information [17]. The speed of information processing at the hardware level also increases with the use of FPGA architecture [18]. This allows accurate tracking of flying objects. When using satellites, it is necessary to ensure a large number of operations performed by the optical processor for information processing [19]. The optical system is flexible and easy to use and involves implementation in the assembly programming language.

High requirements are imposed on the IPS used in the military field, one of which is the range of performance from one GFLOPS to ten TFLOPS, so Intel offers various architectural solutions to achieve the specified performance [20]. For example, the performance of a batch processing system is diagnosed by throughput [21].

Thus, IPSs are designed to process ARP information, which can be pre-analyzed and then diagnosed with specialized tools. An example of specialized tools is the numeral system, which is based on sections of mathematics: number theory, theory of computing processes and systems, theory of failure-resistant coding [22]. The analysis of existing methods of increasing the speed and reliability of processing various types of information showed that currently no new structural solutions are used in the creation of the IPS by using alternative numeral systems. Continuation of research in this area and the development of new numeral systems can contribute to the further development of fast and efficient digital devices for the automation of various processes, including IPS.

The search for new numeral systems for the construction of digital ARP devices is a global problem today, as it allows for the creation of high-speed computing systems [23]. The development of the Internet of Things gives rise to the creation of new numeral systems, where each study involves the selection of a numeral system [24]. For example, it is proposed to solve the problems of the theory of functions using the Cantorian binary-Fibonacci numeral system [25].

Thus, work [26] provides an overview of numeral systems with weighted redundancy, where the advantage of the proposed solution is the possibility of building redundant DACs without a specialized elementary base. The proposed solutions represent the concept of creating information and control systems. For example, in the work [27] the authors proposed information and control system based on the binomial numeral system. The uniqueness of the idea is the minimization of investments in the development of hardware and software solutions, where the binomial numeral system provides fault tolerance, reliability, and speed. The indicated advantages are also evidenced by the results of research [28], but with the use of a non-positional numeral system.

In contrast to the work [27], the research [29] involves the process of creating a special multiplication processor using a two-dimensional numeral system. Thus, a comparative analysis of the proposed and existing solution showed the advantage of the matrix calculation system for multiplication operations, where the time spent on the specified operations is more than 2,000 and more than 20,000 seconds, respectively.

PNS researched in [30] are used in the IPS to transmit, process, and store information. The uniqueness of the proposed solution is the possibility of detecting errors during data manipulation. In contrast to the work [30], the authors of the research [31] proposed not only a model, but also implemented schematic solutions and typical modules of an arithmetic device. The proposed solutions allow more effective detection of errors.

However, most of the considered IPSs are implemented on the traditional binary PNS, the limitations of which are working with long numbers, where many bits must be used, which complicates IPSs. Other known problems are related to difficulties with representation of decimal fractions, complexity of performing certain operations, redundancy of code structure, inter-bit connections and others. In addition, the proposed positional code structures do not provide for the existence of monitoring and error correction in the dynamics of the IPS computing process [35].

It is also advisable to briefly consider the process of error correction in the IPS of the ARP. The process of correction (detection and correction) of errors in the information code structure of the ARP data consists of the following main stages:

- data control (the process of detecting the fact of the presence of an error in the code structure);
- data diagnostics (localization of the location of errors with a given depth of diagnostics);
- correction of errors in the code structure of the data (restoration of distorted data, usually presented in the form of a code, that is, restoration of a distorted number and obtaining a correct number).

Control and diagnostics are designed to ensure the search for emerging faults (errors) in the IPS of the ARP with the aim of its further elimination. By fault, let's mean a violation of the normal technical condition of the IPS of the ARP, which is determined at the stage of development of the object and is reflected in the rules of its operation, which are fixed in the technical documentation.

Control is a check of the IPS of the ARP for the presence of a failure. The result of the control is the choice of one of two alternative answers: positive - the object is operational or negative – the object is inoperable.

A failure is such a violation of the object's performance when a persistent fault appears in it. A fault is considered persistent, which, having appeared, cannot be eliminated by itself. Violation of the operational efficiency of the IPS of the ARP is manifested in its incorrect (not foreseen in advance) functioning (at least in one of the operating modes allowed by the rules). Thus, the failure is an event, the occurrence of which makes it impossible to further use the IPS of the ARP for its direct purpose until the fault that has appeared is not eliminated.

Diagnostics is the search for faults (errors) that led to the failure of the IPS of the ARP. The result of the diagnosis is the determination of the specific location and nature of the found faults or the indication of those parts in which these faults occurred.

Methods of monitoring the performance of the IPS of the ARP are closely related to its operation as a service object. How rationally it is chosen will depend on the efficiency

of the operational maintenance of the IPS of the ARP. When designing such a complex system as IPS of the ARP, and its software, one should take into account the peculiarities of operation and the effectiveness of certain methods of performance control in the process of operation of the IPS of the ARP. The necessary operational characteristics of the IPS of the ARP should be included as initial parameters in the design process of all elements of the IPS of the ARP.

Let's consider the main classification of automatic methods of control and diagnosis of the IPS of the ARP. During hardware control (diagnostics), the search for faults in the device (or its individual parts) is carried out by specially provided equipment, which is not needed if there are no failures. This equipment during external control (diagnostics) is not included in the controlling (diagnosing) device, and when internal it is considered as additional (in relation to the main one). The features of hardware methods are the high speed of fault finding and the possibility of fixing unstable faults, and the disadvantage is the presence of additional (excessive) equipment.

During software control (diagnostics) with the help of special programs, the following modes of automatic operation are organized, in which the blocks and elements of the device mutually check each other. Software control and diagnostics use the device's own functionality and are therefore internal. This is its disadvantage, because the device or its individual parts do not work according to its direct purpose. However, the advantages of software control methods (diagnostics) are the possibility of its constant improvement (by changing programs) during operation, when the accumulated experience suggests new, more effective technical solutions, and hardware modifications are practically excluded.

Hardware and software control combines the advantages of both control methods discussed above and is largely free from its disadvantages. With such control, a part of the device's equipment in certain time periods specified by the program switches from solving the main task to monitoring the correct functioning of another part of the equipment, which continues the solution of the task. In this case, only part of the device does not perform its intended purpose.

Depending on what part of the device's working time is devoted to finding faults, as well as on the means involved, control and diagnostic methods can be divided into operational and test.

During operational control (diagnostics), the search for faults is carried out by specially designed technical means during the entire time of operation of the device.

In contrast to this, test control (diagnostics) is carried out by switching the device (or its individual parts), at certain time intervals, into special auxiliary modes of operation. These modes are not related to the direct functional purpose of the device and are entered only for troubleshooting. Two characteristic pieces of equipment are always involved here. One is controlled (diagnosed), acting as an object of control (diagnosis), and belongs to the device in which fault finding takes place. The other part is controlling (diagnostic) and is not necessarily included in this device. This part of the hardware, on which the functions of automatic control of the fault finding process rely, is usually called the base.

In the process of test control (diagnosis) with the help of hardware and software included in the base, the formation and issuance of a certain number of input sets to the inputs

of the object of control (diagnosis) is carried out, as well as the reception and analysis of the output sets received at the outputs object. Each input (output) set is a completely specific combination of signals at the inputs (outputs) of the object. On the basis of the analysis of the initial sets produced in the database, carried out according to formal rules (for example, by comparison with reference initial sets), control results (diagnostics) are determined. Data on the results of control and diagnostics are used to implement measures to eliminate faults.

Experience shows that monitoring is usually easier than diagnosis. In addition, the really emerging limitations on the practicality of control and diagnostic procedures lead to the fact that with the increase in the number of controlled (diagnostic) equipment, the solution of problems of finding faults becomes more complicated. All this naturally affects the technical solutions used in practice. In particular, for example, the hardware-software method of troubleshooting is often preferred with the following combination: operational hardware control (during the operation of the device) plus test software diagnostics (in special modes not related to the direct functional purpose of the device).

In the technical implementation of test methods of control and diagnostics, striving for the maximum simplification of fault finding procedures, the following strategy is usually followed. First, control is performed, and then, if a failure is detected, it proceeds to diagnostics. Both control and diagnostics are generally implemented in stages and at each stage fault finding is carried out in the device blocks available for control and diagnostics from the base. After checking and establishing the functionality of certain blocks of the device, it is included in the database. Such expansion of the database is necessary to ensure the search for faults in those units that were initially unavailable for control (diagnosis) [36].

Within the unit available for control (diagnostics), fault finding is organized according to the following principle. Faults that occurred in the block elements are manifested in the form of distortion of the output signals. If the distortion of the signal at the output of some element is the cause of the distortion of the signal at one or another output of the block, then it is said that there is a sensitive path between the corresponding outputs of the element and the block. If the distortion of the signal at the output of the element does not lead to the distortion of the signal at this output of the block, then it is said that there is no sensitive path between the corresponding outputs of the element and the block. So that, during the search process, the fault of the element manifests itself at the outputs of the block in the form of a change in its output set, it is enough to select any of these input sets (at least one such set always exists, otherwise it is not possible to speak of a fault), in which case this fault will be expressed in the form distortion of the signal at the output of the failed element, and there will be a sensitive path between the output of this element and at least one output of the block.

In the process of troubleshooting, by properly choosing the sequence of input sets, it provides:

- during control – that each of these faults manifests itself (appeared) at least once;
- during diagnostics – so that different faults manifest itself in different ways.

CHAPTER 2. JUSTIFICATION OF THE IMPORTANCE TO CREATE INFORMATION PROCESSING SYSTEMS BASED ON THE USE OF A SYSTEM OF RESIDUAL CLASSES

The decisive role of the data processing process (collection, input, recording, conversion, reading, storage, registration) in the automated systems of the state's defense capability, one of which is the developed ARP, is played by IPS.

The effectiveness of the ARP systems is completely determined by the technical capabilities of the IPS. In this regard, there is a need to set requirements for the IPS of the ARP, focused on the processing of digital information and digital signals. The requirements of the IPS of the ARP include:

- adaptability to the class of tasks (to the mathematical model);
- functioning IPS of the ARP in real time;
- high user performance of real-time information processing;
- high reliability (failure tolerance) of operation and reliability of calculations; the possibility of parrying failures;
- failures (adaptation to failures and failures that occurred during the operation of the IPS), that is, the IPS should have the property of survivability and failure resistance;
- ensuring the specified weight and size characteristics, etc.

The analysis of the types of operations included in the algorithms of the IPS of the ARP systems showed that effective mathematical models of such systems are models based on the application of the apparatus of the theory of Galois fields, finite fields, etc. Such models have a number of significant advantages: the structure of the digital signal is more fully taken into account; the technical implementation of a mathematical model on digital means of information processing is facilitated; the application of the mathematical apparatus of finite Galois fields allows us to approach the solution of the problem of digital signal processing and synthesis of the IPS of the ARP from a single point of view. Along with the obvious advantages of models of algebraic systems of finite Galois fields, there are also disadvantages, the main of which are the following: lack of a clear physical meaning of the results of intermediate calculations; the problem of creating IPS of the ARP for the effective implementation of field and ring structures, in particular, the creation of separate functional blocks and nodes of the IPS processing digital signals. The methods of synthesis of the IPS of the ARP, defined over abstract systems of algebra, are partially developed. Its further improvement, as well as the development of new principles, methods and models for the creation of the IPS of the ARP, synthesis of its functional blocks and nodes is a very urgent and important task.

One of the main effective ways to achieve high efficiency in the functioning of the IPS of the ARP is to improve, first of all, such characteristics as the productivity and reliability of processing large amounts of information in real time, as well as the reliability of its operation [37]. Thus, today, the development of super-productive and reliable real-time IPS is under the special control of heads of state and government and is classified as a

strategically important and pressing problem in the scientific and technical development of automated defense systems of the state, which confirms the relevance and importance of research conducted in this direction.

The perspective of the development of the IPS of the ARP in terms of increasing reliability and fault tolerance is aimed at the application of separate structural redundancy at the level of individual functional nodes: memory device, operating device, peripheral units with the simultaneous use of software control methods. This circumstance requires an additional amount of equipment for IPS, which worsens the technical and economic characteristics of the ARP. According to the foreign press and the available data, the main feature of the architecture of modern IPS of the ARP is the decentralization of the management and information processing subsystems served by it. As a result, such information processing complexes use the hierarchical principle of building multiprocessor systems, which also requires a significant increase in the number of IPS equipment and, at the same time, does not fundamentally solve the problem of ensuring the required degree of reliability and resistance to failures. So, for example, the main method used to increase the reliability and resistance to IPS failures is the use of dynamic structural redundancy at the level of tripled majority channels of information processing with the possibility of restructuring the structure in the process of solving algorithms. At the same time, a high degree of fault tolerance can be ensured in the short-term (initial) time interval of the operation of the ARP.

The development trend of the IPS of the ARP is aimed, first of all, at increasing the reliability, survivability and fault tolerance of functioning, increasing the performance of calculations and increasing the length of the bit grid [38]. This trend is due primarily to the need to improve the accuracy of processing large amounts of information in real time. It should be noted that the resistance to failures of the IPS of the ARP is closely related to the performance of calculations. Indeed, to check the functionality of the IPS information processing channels, ARP uses control tests that are carried out at certain time intervals specified in the IPS frame. The greater the time allocated to control the information processing channel, the greater the degree of reliability of the IPS of the ARP control, but the less time allocated to processing input information. Thus, with an increase in the reliability and fault tolerance of the IPS, the productivity of information processing significantly decreases.

Modern IPS of the ARP, created taking into account the use of the PNS, are being improved mainly with the help of miniaturization of its elemental base and the creation of multiprocessor computing systems. The transition to VLSI chips on a silicon basis significantly improved the main characteristics of the IPS and, first of all, performance, reliability, dimensions, and power consumption. However, the miniaturization of the elemental base based on the use of the VLSI chips, in addition to unresolved problems (minimization of intercircuit connections between VLSI chips, reduction of the number of applied types of the VLSI chips, etc.), has practically reached its limit. Currently, the size of the topological elements included in the VLSI chip is approximately $0.5\div 0.1\text{ }\mu\text{m}$. The further reduction of the size of the elements included in the VLSI chips causes significant difficulties, which consist primarily of the following: solving the problem of control and diagnosis of the VLSI chips; the installation of small crystals reduces some indicators of reliability and failure resistance of the IPS, worsens economic indicators; when reducing the size of the VLSI

chip elements, there is a need to reduce the operating voltages, for which the limit may be thermodynamic processes occurring in it, for example, inherent noises, at the same time, the silicon-based semiconductor material itself has the maximum allowable values of the electric field strength, which also limit sizes of transistors.

At the same time, in connection with the complexity and scale of the country's problems to be solved during the war, the solution of military tasks, the tasks of data processing under time limits, etc., the requirements for increasing reliability and increasing both system (productivity, that is achieved when solving a set of user tasks), and user (productivity that is achieved when solving one single task) productivity of the IPS of the ARP are constantly increasing. This circumstance dictates the need for further research into ways to increase system and especially user productivity (reducing the time to solve a given specific task), as well as the reliability of the IPS of the ARP. In this regard, two main global trends in solving this dual problem are obvious:

- creation of a new elemental base of computer technology;
- creation of a computer system of innovative architecture, which involves the implementation of holographic principles of information processing.

The complexity, scale and scope of management tasks solved by ARP requires the expansion of the functions and capabilities of the IPS, which necessitates an increase in the number and complexity of computer equipment and systems, as well as the complication of its mathematical and software. This, in turn, makes it necessary to take additional measures to ensure the high reliability and fault tolerance of the operation of the IPS, as well as its high survivability.

This circumstance necessitates the development and application of fundamentally new methods of increasing the productivity and reliability of the IPS of the ARP, which are based on the use of new principles and ideas. In particular, information processing methods based on the application of codes presented in the non-positional numeral system in residual classes. This scientific direction is the development, on the one hand, of the idea of multi-residue coding of data and, on the other hand, of cluster systems of information processing in the positional numeral systems.

The theoretical foundations of the construction of a non-positional numeral system in residual classes are the development of sections of the theory of comparisons that are widely known in number theory. The results of the scientists' research indicated the possibility of over-coding of integers using a set of residues $\{u_j\}$, which are formed from the division of these numbers into mutually pairwise simple natural numbers $\{b_j\}$, ($j = \overline{1, g}$), called bases (modules) of the SRC, which is also called modular arithmetic [39]. A significant contribution to the development of the theory of non-positional coding in SRC and its use for the construction of IPS was made primarily by scientists: I. Ya. Akushskii, D. I. Yuditskii, V. A. Torgashov, V. A. Krasnobayev, P. V. A. Mohan, A. R. Omondi and others.

The main advantage of the SRC is the possibility of organizing the process of high speed implementation of the following modular operations: arithmetic operations of addi-

tion, subtraction and multiplication; operations of logical addition, subtraction and multiplication modulo two; division of whole numbers, etc. One of the shortcomings of SRC lies in the fact that there are daily simple signs that the result of an operation is outside the

operating range $[0, P)$, where: $P = \prod_{j=1}^g b_j$ – the operating range of the SRC; b_j – j -th base

(module) of the SRC; g – number of working bases (modules) of the SRC. Therefore, based on the above, in order to achieve high reliability of operations in the SRC, additional time is required for the implementation of the data control and diagnostics process [40]. However, control, diagnostic and correction operations are non-modular operations that are technically and time-difficult (significant hardware and time charges) to implement in the SRC.

That is, with the proven fact of the effective use of the SRC to create high-performance IPS, the time for implementing methods and algorithms for data control (in relation to the time of information processing) is very significant, which reduces the overall efficiency of using non-positional code structures.

It was the unsolved problem of significantly reducing the time of data control in the data control system operating in the SRC, taking into account the requirements for the performance of information processing of the ARP, that determined the goal, the general scientific and technical task of this monograph.

CHAPTER 3. FORMULATION OF PRINCIPLES FOR CONTROL OF NON-POSITIONAL CODE STRUCTURES IN THE SRC

The principles of controlling non-positional code structures in the SRC are the same as compared to positional numeral systems. However, as a result of using the properties of the SRC, which affect the features of the construction and functioning of the IPS and the very structure of the code in the SRC, the following principles of data control are formed:

- the principle of authenticity of control;
- the principle of continuity of control;
- the principle of promptness of control.

We also note that the number of control equipment takes approximately 20-25% of the total number of hardware of the ARP.

When choosing control methods, the main attention should be paid to the ability of this control method to detect errors, as well as to the amount of equipment and time spent on control.

As noted earlier, the software methods for controlling the correctness of calculations are designed to check the correctness of the implementation of the calculation process in different operating modes of the IPS and the correct functioning of all devices of the IPS. These methods are based on the inclusion in the software of special control programs or additional ratios in the general algorithm.

Software-logical control based on the use of information redundancy and designed to check the correctness of the implementation of the computing process. Informational redundancy is ensured by the inclusion of additional ratios in the general algorithm, which make it possible to identify and correct errors that occur during calculations [37].

Let's consider the most common methods of software and logical control.

Method of double calculation with comparison of results. Its main advantage is ease of implementation. Its essence is that the entire working program is divided into separate parts and after the execution of any stage of calculations, a control summation of all commands, intermediate and final results of the stage being controlled is made. The checksum is memorized and recalculation of this stage is performed with subsequent checksumming. Both checksums are compared. When comparing, the next stage of calculations is performed. In case of disagreement, the third miscalculation of this stage is made. If the third checksum coincides with one of the previous ones, the next stage of calculations is performed. Otherwise, a signal is given about work failures in IPS. This method also has disadvantages: it increases the algorithm implementation time, which is permissible only in the presence of excessive speed of the IPS and allows detecting and eliminating only random errors caused by system failures. When organizing control by the method of double calculation, it is necessary to correctly divide the algorithm into controlled stages. As the main criterion for breakdown, it should be taken to ensure the necessary probability of detecting an error with a minimum time spent on control. Studies have shown that there

are an optimal number of controlled parts of the algorithm, in which the time spent on control is minimal.

The experience of operation of the IPS of the ARP shows that the flow of random failures can be taken as simple. Let's denote the intensity of the flow of random failures by λ_f , the time to solve the problem by t_p , the number of controlled parts by n . Then the time to implement one controlled part of the algorithm will be determined as:

$$T = \frac{\lambda_f \cdot t_p}{n}. \quad (1)$$

It should be taken into account that when organizing control by the method of double calculation, additional time is spent on each part of the task being controlled, for control summation, comparison of control sums, decision-making on the third calculation or continuation of calculations, which in general leads to significant time losses when implementing this method.

The method of control ratios allows determining not only errors that appear due to random disruptions, but also errors that appear due to failures. The essence of this method is that various mathematical ratios are included in the general algorithm, which allows checking the correctness of the solution to the main problem by implementing it. When the control ratios are performed with the specified accuracy, a further solution of the main problem is carried out. If the control ratios are not fulfilled, either this part of the task is repeated, or the IPS operation is stopped. The control ratio method can provide significant time savings compared to the double calculation method.

The method of the truncated algorithm allows detecting and eliminating errors due to random disruptions and systematic failures, if the truncated algorithm is significantly different from the main one. This method assumes the availability of a simplified algorithm for the main problem. The simplified algorithm must be smaller than the basic one. The implementation of the truncated algorithm together with the main one and the coincidence of the results within the specified accuracy allow judging the correctness of the computational process.

The method of logical analysis of decision results allows identifying both random and systematic errors. Its essence is to compare some parameters of the problem and its increments, calculated during the solution of the problem, with the previously known limits of its change. The method is used if the laws of changing some parameters are known in advance.

The substitution method consists in the fact that after receiving a number of sought-after tasks, the reverse task is solved. The found values of the unknowns are selected as the initial data and some values are determined, which were used as initial data during direct calculations. Then these values are compared with the initial data during direct calculation. Coincidence within the specified accuracy indicates the absence of errors in calculations. For example, when solving systems of algebraic equations, the roots $y_1 \parallel y_2 \parallel \dots \parallel y_k$ those obtained in the calculation, can be taken as initial data; as unknowns, k are the coefficients determined during the inverse solution of the problem; $\parallel$ is the operation of concatenation, the operation of gluing (merging), which is used in the SRC to represent a number as a set

of residues from division by the corresponding bases. Comparison of the obtained coefficients with the existing ones, within the specified accuracy, indicates that the system is solved correctly. A similar method can be used when solving systems of differential equations.

When developing the general algorithm of the IPS of the ARP, it is necessary to use the most effective methods of controlling the correctness of calculations, which allow to significantly increase the reliability of information processing with minimal expenditure of machine time.

All the considered methods of control of calculations are effective only under the condition of the correctness of the implementation of the IPS of the ARP programs.

Control of the execution progress of the IPS of the ARP programs: each program that implements one or another mode of operation of the IPS consists of separate sub subprograms by the dispatcher program. The correctness of the program execution is determined by: control of the sequence of inclusion of subprograms; control of the duration of subprograms of the generated program; control of transitions and interruptions of the program.

Control of the sequence of inclusion of subprograms: the operating mode of the IPS of the ARP and the system is ensured by a corresponding program consisting of separate subprograms S_j executed in turn. The method of control is as follows. During the time t_j , subprogram S_j is activated at least once, and as a result of each execution of the subprogram, some parameter $P_j(t)$ stored in RAM changes. By checking the $P_j(t) \neq P_j(t + t_j)$ ratio, it can be established that subprogram S_j was executed.

For each mode of operation performed by IPS of the ARP, connections between separate subprograms are known in advance. Determinism of connections between programs is used to control the sequence of its execution. In this case, each subprogram, when executed, fixes in a certain memory cell the conditional code previously attached to this subprogram. The execution of the next subprogram begins only after the analysis of the conditional code written during the execution of the previous subprogram.

Control of the duration of operation of subprograms of the generated program: assumes control of the duration of operation of individual parts of the program and allows detection of program implementation violations due to looping and other reasons that lead to an increase in the implementation time of individual program subprograms. For this purpose, relative time counters designed for counting time intervals are used. In this case, certain restrictions are imposed on the duration of t_j execution of subprogram S_j . At the beginning of each subprogram, a code corresponding to the permissible relative duration of execution of this subprogram is entered into the relative time counter by a special command. At each implementation of the subprogram S_j , one is subtracted from the content of the relative time counter. If the counter has a relative time of zero, an error signal is generated, which causes the program to be interrupted and the transition to the error analysis subprogram. Otherwise, there is a transition to the execution of the next subprogram.

Control of the correct execution of transitions and interruptions of the program is carried out using conditional and unconditional control transfer commands and is based on

program blocking of the error signal. The idea behind this control is that before a jump is executed by a special command, an error signal is sent to the address modification and jump execution chain, the arrival of which can be blocked by blocking commands located in all places of the program where the jump occurs [41].

If the transition is not performed correctly, the error signal will not be blocked and will cause an interruption and activation of the failure analysis program. This method provides a high probability of detecting both random and systematic errors of any multiplicity, but requires additional equipment and special commands in the program.

Interruption of the program is a characteristic feature of the work of the IPS of the ARP, which implements its algorithms on a real-time scale. During the operation of the IPS of the ARP, depending on the operating mode of the system and the volume of incoming and outgoing information, numerous interruptions of the program are made, amounting to hundreds of interruptions per second.

To control the correct execution of program interruptions, the considered method of program blocking of the error signal is often used. The only difference is that the generation of the error signal is carried out by a circuit, and the interruption can be anywhere in the program. Blocking of the error signal is carried out by one of the first instructions of the jamming subprogram. Control of the transition to the main program after an interruption is carried out by checking the correctness of the restoration of the state of the main results of the registers and memory elements of the IPS of the ARP, which were used by the jamming subprogram. For this purpose, the method of multiple storage of variable information in the machine's memory and its subsequent comparison is used.

An error signal is generated when the content of at least one register or memory element is inconsistent.

In the case of hardware control, which provides control of the machine or its individual devices with the help of additional equipment included in the IPS of the ARP, module control is common. This control is that comparisons of a kind are used: $y \equiv \alpha \pmod{b}$.

With this control, the value of the control code α is used as redundant information. There are two types of module control: numerical and digital.

With digital control by modulo, the control code is formed as a residue from dividing the sum of the digits of the number y by the module b . With numerical control by modulo, the control code is formed as a residue from dividing the number y by the module b . For example, if $b = 3$, then the comparison (1) can be written as follows:

with digital control	with numerical control
$y = 101010 \equiv 00 \pmod{3}$	$y = 101010 \equiv 00 \pmod{3}$
$y = 101001 \equiv 00 \pmod{3}$	$y = 101001 \equiv 10 \pmod{3}$
$y = 111010 \equiv 01 \pmod{3}$	$y = 111010 \equiv 01 \pmod{3}$

The codes 00, 00, 01 and 00, 10, 01 appear here as control codes α .

When using the binary numeral system for $b = 2$, digital control modulo is reduced to parity (odd) control. However, digital control, for example, when checking the correctness of the addition operation, requires counting the units of transfer. As a result, it is used mainly to control the correctness of code transmission and the correctness of information storage in memory.

It is known from number theory that comparisons are valid for numerical control:

$$\begin{cases} \sum_{j=1}^g y_j \equiv \sum_{j=1}^g \alpha_j \pmod{b_j}, \\ \prod_{j=1}^g y_j \equiv \prod_{j=1}^g \alpha_j \pmod{b_j}. \end{cases} \quad (2)$$

The given systems of expressions (2) allow you to control the execution of addition and multiplication operations.

Hardware control by module provides reception of error signals that occur when the main and control equipment faults. In this case, random and systematic errors are recorded. However, hardware control does not always provide the necessary degree of verification of the correct functioning of the IPS of the ARP. Therefore, the most rational organization of the control system is the combined control method, which combines hardware and software control methods and satisfies all the requirements for control systems [42]. The main problem of using a combined control method is to determine the optimal ratio of software and hardware control methods, which depends on the operating conditions and application of the IPS of the ARP.

CHAPTER 4. RESEARCH OF CORRECTIVE POSSIBILITIES OF CODES IN THE SRC

In general, data error correction requires that the code structure has some correction capability. For this, it is necessary to introduce a certain information redundancy, that is, to apply the method of information redundancy. This fully refers to the non-positional code structure in the SRC [37].

Numerous studies have substantiated the possibility of building IPS, in which, due to special coding, immunity against a wide variety of signal information distortions can be created. The point of view was absolutely clearly formed that the struggle for high reliability of information transmission, that is, for the reliability of information restoration at the receiving end of the transmission line, should be conducted not so much by improving the technical means of information transmission, where any possible increase in reliability is achieved at a high price and sometimes requires the development of complex protective measures, such as the use of information encoding methods that would be resistant to possible accidental distortions of information, meaning by this the ability, through the appropriate processing of received information, to exclude disturbances introduced into it, to clear it of errors and to achieve full compliance with what was sent from the transmission end of the line.

While increasing the reliability of information transmission by technical means, even if we ignore the economic side of the issue, is limited by the level of development of technical means and any achievements in this area require new technical solutions, the use of special code systems for the same purpose does not contain any fundamental limitations. Moreover, when choosing the appropriate code that has the necessary corrective ability, it is possible to significantly lower the reliability requirements of the information transmission lines itself, make it simpler and cheaper.

For computing devices, the use of special coding methods is dictated by an urgent need. After all, any IPS is itself a system of transmission and processing of information. There is a constant circulation of information in the IPS of the ARP. Although the machine does not have long transmission lines, information circulates with great speed and in large quantities on the relatively short lines that exist in it. If we accept some conventional unit, for example, passing one centimeter of the path with one binary bit, then in these conventional units, the work of one computing machine of average performance for a fixed time interval for information transmission will be comparable to the work for the same interval of a number of large transmission lines.

Therefore, even from the point of view of information transfer only, during the development of computing tools, there is an important task of ensuring the reliability of the entire colossal flow of information. After all, in the IPS, in addition, the reliability of arithmetic and logical processing of information must also be ensured. Practically, without the use of special coding methods, ensuring reliability in the IPS of the ARP is achieved by double calculation to identify the correctness or incorrectness of the results of problem solving and by triple calculation in the case of a detected discrepancy to choose the correct

result based on matching data. This way of ensuring reliability reduces the actual performance of the machine by at least half. It is clear from this that ensuring reliability by any methods, other than the specified recalculations, is directly and directly related to increasing the productivity of the IPS of the ARP.

Each special code, which is required to have the ability to detect and correct an error, is characterized by the presence of two groups of numbers – informational and control. The information group includes numbers that constitute the numerical value of the coded value, and the control group includes numbers that are additionally entered for the purposes of detecting and correcting possible distortions during transmission. These additional digits are excessive from the point of view of the numerical value of the quantity and lengthen the total length of the code, which, of course, somewhat reduces the bandwidth of the channel in serial transmission and increases the number of channels in parallel transmission. However, these circumstances should be compensated by those opportunities that deliver excessive numbers for detecting and correcting errors.

In general, data error correction requires that the code structure has some correction capability. For this, it is necessary to introduce a certain information redundancy, that is, to apply the method of information redundancy, by expanding g information bases $(b_1, b_2, \dots, b_g)$ with k control bases $(b_1, b_2, \dots, b_g, b_{g+1}, \dots, b_{g+k})$. This fully refers to the non-positional code structure in the SRC.

For any arbitrary SRC, the amount of redundancy is $R = P_0 / P$, where $P = \prod_{j=1}^g b_j$ – number of information code words for a given SRC or as the operating range of SRC (which takes into account only the available g information bases) was previously called; $P_0 = \prod_{j=1}^{g+k} b_j$ – the total number of code words for a given SRC (which takes into account only the available g information and k control bases); unambiguously defines the corrective capabilities of a non-positional error-correcting (failure-resistant) code.

Correction codes in the SRC can have any values of the minimum code distance $C_{\min}$. It depends on the value of the redundancy value R [43]. The relationship between the redundancy R of the correction code, the value of $C_{\min}$, and the number of k control bases of the SRC is as follows. The correction code has the value $C_{\min}$ of the minimum code distance if the degree of redundancy R is not less than the product of any $C_{\min} - 1$ bases of the SRC. That is, on the one hand, we have that $R \geq \prod_{j=1}^{C_{\min}-1} b_j$, and on the other hand –

$R = P_0 / P = \prod_{j=1}^{g+k} b_j / \prod_{j=1}^g b_j = \prod_{j=1}^k b_{g+j}$. In this case, it is legitimate to claim that $C_{\min} - 1 = k$ or the following expression can be written:

$$C_{\min} = k + 1, \quad (3)$$

where k is number of control bases of the SRC.

There are two approaches to the solution of the problem of providing the non-positional code structure in the SRC with the necessary corrective properties.

The first approach. Knowing the requirements for the corrective properties of the non-positional code structure in the SRC, for example, by the number of detected N_{det} or corrected N_{cor} errors, introduce, due to the number k or size $\{b_{g+k}\}$ of control bases, the necessary information redundancy R . Redundancy R determines the minimum code distance C_{min} of the non-positional code structure in the SRC [4].

Then, according to the theory of failure-resistant coding, for an ordered ($b_j < b_{j+1}$) SRC we have that:

$$N_{\text{det}} \leq C_{\text{min}} - 1, \quad (4)$$

$$N_{\text{det}} \leq k; \quad (5)$$

$$N_{\text{cor}} \leq \left\lfloor \frac{C_{\text{min}} - 1}{2} \right\rfloor, \quad (6)$$

$$N_{\text{cor}} \leq \left\lfloor \frac{k}{2} \right\rfloor. \quad (7)$$

The second approach. With a given non-positional code structure $U_{\text{SRC}} = (u_1 \parallel u_2 \parallel \dots \parallel u_{j-1} \parallel u_j \parallel u_{j+1} \parallel \dots \parallel u_g \parallel \dots \parallel u_{g+k})$ (with a given value of k), the corrective capabilities (defined by the value C_{min}) of the code in the SRC are determined according to expressions (5) and (7).

Note that if the ordered SRC is expanded by adding k control bases to g information bases (modules), then the minimum code distance C_{min} of the error-correcting (failure-resistant) code increases by the amount k (see expression (3)).

It is also possible to increase the value of C_{min} by reducing the number of g information bases (that is, reducing the redundancy R of code in the SRC), that is, by switching to calculations with lower accuracy. It is obvious that there is an inversely proportional relationship between the corrective capabilities of error-correcting (failure-resistant) codes R and the accuracy A of calculations the SRC. The same IPS can perform arithmetic and other operations with high A accuracy, but little correction ability R , or with less A accuracy, but with a higher R correction ability for monitoring, diagnosing and correcting data errors, as well as with higher data processing speed (the execution time of basic operations in the SRC is inversely proportional to the number of g information bases).

Assessing the effectiveness of using the SRC to increase the efficiency of data control of the ARP significantly depends on the specific structure of the IPS and on the element base used. It also depends on the requirements for accuracy, speed, reliability and reliability of solving telecommunications network problems. At the same time, the reliability of the obtained calculation result depends on the organization of control, diagnostic and error correction procedures. To do this, let us consider the basic concepts and definitions of the theory of error-correcting coding in the SRC [43].

The relationship between the minimum code distance $C_{\min}$, i.e. the smallest distance between code words and its correcting capabilities is established by the following two well-known theorems.

Theorem 1. The correcting code in the SRC can detect all sets of z or fewer errors only if the minimum code distance of the code is greater than z , i.e.:

$$C_{\min} \geq z + 1. \quad (8)$$

Theorem 2. The correcting code in the SRC can correct all sets of w or fewer errors only if the minimum code distance of the code is greater than twice the number of errors, i.e.:

$$C_{\min} \geq 2w + 1. \quad (9)$$

Let's show the need to fulfill condition (9) to correct w -fold errors. If the minimum stake distance is less than $2w + 1$, then there are at least two code words U_1 and U_2 , the difference of which has a weight not exceeding $2w$. Accordingly, it is always possible to find two error vectors θ_1 and θ_2 such that $U_1 - U_2 = \theta_1 - \theta_2$. Consequently, it is impossible to unambiguously obtain a code word from the value of the distorted vector, which is what needed to be proven.

From Theorems 1 and 2 it follows that the correction code in the SRC, correcting any w errors and, in addition, detecting any $w + 1$ errors, must have a minimum code distance equal to $2w + 1$. Thus, by determining the minimum code distance, it can get an idea of its corrective capabilities. It should be taken into account that the minimum code distance is a rather rough characteristic that does not fully reveal the structure and capabilities of the code. In particular, if the distance between the majority of code words exceeds the minimum, then such a code can be used to detect or correct a significant portion of errors of higher multiplicity than the multiplicities defined by Theorems 1 and 2. Therefore, we can assume that the minimum code distance of the code allows us to establish only a guaranteed number of detected or corrected errors. Note that the minimum code distance of a code can be determined if the weights of the code words are known.

Theorem 3. The minimum code distance of the correcting code in the SRC is equal to the minimum weight of non-zero code words if the plural L does not contain numbers of opposite signs [4].

It follows from the Theorem 3 that the minimum code distance can be determined if the weights of the code words are known.

Consider some vector $U = (u_1 \parallel u_2 \parallel \dots \parallel u_{g+k})$ whose components are natural numbers that satisfy the condition: $0 \leq u_j \leq b_j - 1$, where $j = \overline{1, g+k}$; $b_1, \dots, b_{g+k}$ – fixed natural numbers, bases (modules) of the SRC. It is obvious that the number of different (that is, differing by at least one component) vectors of this type is equal to the product

$$P_0 = \prod_{j=1}^{g+k} b_j = b_1 \cdot b_2 \cdot \dots \cdot b_{g+k} \quad (\text{the letter } P_0 \text{ also denotes the set of all vectors of a similar})$$

type, i.e. $U \in P_0$). Thus, depending on the context, the symbol P_0 means either the set of vectors U or the number of elements of this plural.

On the other hand, consider a plural L containing L integers U such that if any two numbers U_1 and U_2 belong to the plural L , then any integer lying between the numbers U_1 and U_2 also belongs to this plural. Let's assume that the composition of the plural L necessarily includes zero.

Any number from the plural L can be represented in the SRC with a common base $P = [b_1, \dots, b_g]$, if $L \leq P$. Each number $U \in L$ represented in a given SRC can be associated with a certain vector $U' \in P_0$, but the converse statement is true only if $P = L = P_0$. If this condition is met, we will talk about the non-redundant representation of numbers in the SRC.

It is obvious that if the bases of the SRC are not mutually prime, then the representation of numbers in such a SRC is always excessive, since $P < P_0$. For the SRC with mutually prime bases $P = P_0$ and therefore the question of redundancy in the representation of numbers depends on the ratio between L and P . The degree of redundancy in the representation of numbers in the SRC is called the value $R = P_0 / L$. Redundancy in the representation of numbers in the SRC can be used to detect and correct errors that occur in the process of storing, transmitting or transforming information.

A corrective code in the SRC is a subplural (subset) K of the plural P_0 consisting of L different vectors U' , each of which corresponds to one and only one number $U' \in L$. Since the plurals K and L contain the same number of elements, each number $U \in L$ corresponds to one and only one vector $U' \in K$. The vectors belonging to the code will also be called code words. The correspondence between vectors $U' \in P_0$ and numbers $U \in L$ can be established in various ways. However, the properties of the codes practically do not depend on the choice of one or another method, and are mainly determined only by the numbers L , P and P_0 . Therefore, in what follows we will assume that the number $U = \{u_1 \parallel u_2 \parallel \dots \parallel u_g\}_P$ corresponds to the vector $U' = \{u'_1 \parallel u'_2 \parallel \dots \parallel u'_g\}$ if and only if $u_j = u'_j$; for any $j = \overline{1, g}$. Therefore, $U' = \{U\}_P$.

Depending on the ratio between the values of L , P and P_0 in the SRC, all correction codes can be divided into three main classes.

The first class of codes of SRC is R-codes. In the SRC, an R -code is a correction code whose vectors correspond to numbers represented in the SRC with mutually prime bases. These codes can have any minimum code distance depending on the degree of redundancy R , and, as follows from the following Theorem 4, for any given SRC, the value R uniquely determines the corrective capabilities of the code.

Theorem 4. The corrective R -code has a minimum code distance $C_{\min}$ if and only if the degree of redundancy R is not less than the product of any $C_{\min} - 1$ bases of the given SRC:

$$R \geq \prod_{j=1}^{C_{\min}-1} b_j. \quad (10)$$

R -codes are most suitable for use in the processing of data presented in the SRC, as the volume of representation of code words is sufficiently wide. For example, for R -code, the range of representation of a non-positional code structure in the SRC with bases will $b_1 = 2, b_2 = 3, b_3 = 5$, be from 0 to 29 ($b_1 \cdot b_2 \cdot b_3 - 1 = 2 \cdot 3 \cdot 5 - 1 = 30 - 1 = 29$).

The second class of codes of SRC is linear L -codes, for which there is a fair relationship $L = P < P_0$. The sum, difference, and product of any L -code vectors are code words. Unlike the R -code, in this case, vectors that are not code words cannot be assigned any integers. The first thing to note is that attempting to detect or correct arbitrary symbol distortions using L -code results in redundancy equivalent to reservation. In the SRC, an L -code is a correction code whose vectors correspond to numbers represented in the SRC, which are mutually non-prime bases. There is a relationship between the redundancy R (code correction capabilities), which is equal $R = P_0 / P$ and L -code ($L = P$), therefore, considering expression (10 not mutually) the expression can be written:

$$L = \frac{P_0}{R} \leq \frac{P_0}{\prod_{j=1}^{C_{\min}-1} b_j} = \prod_{j=1}^{\beta - C_{\min} + 1} b_j, \quad (11)$$

where β is the distance between vectors (numbers) in the space P for any SRC.

The restrictions imposed by Theorem 3 on the set L do not apply to L -codes, since in these codes, unlike the other two correction codes in the SRC, the sum, difference, and product of any code words are necessarily code words.

The L -code will be discussed in more detail when describing the developed method for detecting and correcting errors based on the use of this code. But it is worth noting that the main advantage of the L -code is the simplicity of the decoding devices, that is, the technically simple implementation of the operation of decoding non-positional code structures in the SRC. A disadvantage is the small volume of representation of code words.

The third class of codes of the SRC is RL -codes, for which there is a fair relationship $L < P < P_0$. In the SRC, an RL -code is a correction code whose vectors correspond to numbers represented in the SRC, which are mutually non-prime bases.

After considering all three classes of codes in the SRC, let's give an example. Let, for example, there is a SRC given by mutually pairwise prime bases $b_1 = 3, b_2 = 4, b_3 = 5$, since the bases are mutually prime, the condition $P = P_0$ considered above is fulfilled. If $L = 12$, then this SRC corresponds to an R -code, which has $P = P_0 = 3 \cdot 4 \cdot 5 = 60$; $R = P_0 / L = 60 / 12 = 5$. For a SRC given by mutually pairwise non-prime bases $b_1 = 3, b_2 = 4, b_3 = 6, P < P_0$, corresponds to the L -code ($L = P < P_0$), which has $L = 12$; $P_0 = 3 \cdot 4 \cdot 6 = 72$. Finally, a SRC with mutually pairwise non-prime bases

$b_1 = 3, b_2 = 4, b_3 = 5, b_4 = 6$, corresponds to the *RL*-code ($L < P < P_0$), which has $L = 12$; $P = 60, P_0 = 3 \cdot 4 \cdot 5 \cdot 6 = 360$.

Having considered all three classes (*R*-code, *L*-code and *RL*-code) of the SRC correction codes and the main theorems of failure-resistant coding in the SRC, we will consider some general concepts characteristic of all SRC correction codes.

When evaluating the effectiveness of any corrective code, it is necessary to know the relationship between redundancy R and the ability to detect and correct errors. To determine these possibilities, the concept of minimum code distance $C_{\min}$ is most often used, that is, the smallest distance between any two code words.

The code distance $C_{\min}$ between any two vectors (numbers) U'_1 and U'_2 , from the plural P_0 is called the number of components in which these vectors differ from each other. The following properties of this code distance follow directly from the definition:

$$\begin{cases} C_{\min}(U'_1, U'_2) = C_{\min}(U'_2, U'_1); \\ C_{\min}(U'_1, U'_2) = 0, \text{ then and only if } U'_1 = U'_2; \\ C_{\min}(U'_1, U'_2) \geq 0; \\ C_{\min}(U'_1, U'_2) \leq C_{\min}(U'_1, U'_3) + C_{\min}(U'_2, U'_3). \end{cases} \quad (12)$$

A distance that satisfies the listed properties is often called a metric, and the plural of elements in which the metric is given is called a metric space. The value of the distance between different vectors of a large quantity P_0 varies from 1 to g . It is interesting to note that two adjacent numbers U_1 and U_2 (which differ by one) correspond to vectors U'_1 and U'_2 , the distance between which is g for any SRC.

Let's define the operations of adding, subtracting, and multiplying vectors in the space P_0 in the same way as we defined formal modular operations on numbers represented by SRC. The vectors corresponding to the numbers represented in the SRC are simultaneously scalar quantities. Thus, the operation of multiplying a vector by a scalar does not differ from the multiplication of two vectors. Each vector from the set P_0 can be assigned a certain weight. The weight or weight function $W(U')$ of the vector U' is called the number of nonzero components of this vector.

Obviously, the distance between two vectors is equal to the weight of its difference, i.e.:

$$C_{\min}(U'_1, U'_2) = W(U'_1 - U'_2). \quad (13)$$

Let's present several useful properties of weight functions that directly follow from relations (12) defining the metric and expressions (13):

$$W(U'_1 \pm U'_2) \leq W(U'_1) + W(U'_2), \quad (14)$$

$$W(U'_1 \pm U'_2) = (U'_2 \pm U'_1), \quad (15)$$

$$W(U') = W(-U'), \text{ where } -U' = 0 - U', \quad (16)$$

$$W(U'_1, U'_2) \leq \min(W(U'_1), W(U'_2)). \quad (17)$$

The concepts of distance and weight introduced above are very useful in studying the properties of any correction codes.

Suppose that one of the symbols of the code word U' changed its value as a result of some interference. The resulting new (distorted) vector $\tilde{U}'$ is at a distance equal to one from vector U' . Such an error can be detected only if vector $\tilde{U}'$ is not a code word. Therefore, all code words must be separated from the vector U' by a distance greater than one. The greater the distance between code words, the more errors such a code can detect and correct.

By a single (one-time) error in the SRC, we will understand any distortion of one residue u_j of the number U , which refers to any one base (module) b_j . At the same time, we will call any distortion of N residues corresponding to arbitrary N bases (modules) a N -fold error in the SRC. However, in some cases, when considering L -codes, we will use the concepts of single and N -fold binary errors, understanding by it distortions by the symbol of the binary representation of the residues of $u_1, \dots, u_g$. In the future, we will assume that the errors are additive in nature and are uniquely determined by the error vector $\{\theta\}_p$, the weight of which is equal to the multiplicity of the error. The distorted vector $\tilde{U}'$ is obtained as a result of addition (or subtraction) of the code word and the error vector: $\tilde{U}' = U' + \theta$.

The relationship between the minimum code distance $C_{\min}$ and its correcting capabilities is established by Theorems 1 and 2.

The number U corresponding to any code word U is smaller in absolute value than L and therefore cannot be divided by any product of bases (modules) $\beta - C_{\min} + 1$ of the SRC. If the number U is divisible by some bases (modules) b_j , then the corresponding component of the vector U' must be equal to zero. Therefore, the number of zero components of the vector U' cannot be greater and, therefore, the weight of the vector U' is not less than $C_{\min}$. If all numbers U have the same signs, then Theorem 3 implies that d is the minimum code distance of the correction code in the SRC.

Now suppose that the plural L contains L_1 negative numbers. Consider the set of positive integers Q obtained by adding L_1 to each number U , i.e. $Q = U + L_1$. According to the above proof, the set of vectors Q forms a correction code with a minimum distance $C_{\min}$. But the minimum distances of the received and source codes must be equal by construction. Therefore, even in the case of numbers U with different signs, the Theorem 4 is valid.

Among the code words there will be at least two vectors U_1 and U_2 such that:

$$U_1 - U_2 = \prod_{j=1}^{\beta - C_{\min} + 1} b_j, \quad (18)$$

where β is distance between vectors (numbers) U_1 and U_2 for any SRC.

Therefore, the vector $U_1 - U_2$ contains zero components, that is, its weight is equal to $C_{\min} - 1$. Therefore, the minimum distance of the code (in this case, the distance between the vectors U_1 and U_2) is less than $C_{\min}$, which contradicts the condition of the theorem. Therefore, the Theorem 4 is completely proved.

Let's show that the R -code can detect and correct some number of errors of higher multiplicity than the one allowed, according to Theorems 1, 2 and the minimum code distance. Suppose that the minimum code distance of the code is equal to $C_{\min}$, but at the same time there are such bases (modules) of the SRC, the number of which is $C_1 \geq C_{\min}$, such that the product of these modules is less than R . Then any errors in these bases (modules) can be detected. Indeed, the error vector θ must have at least $\beta - C_1$ zero residues. Let's denote the product of the bases (modules) corresponding to the distorted symbols by $\Theta(C_1)$, that is, the non-zero components of the vector θ . Then the number θ is a multiple of the value of $P / \Theta(C_1) \geq P_0 / R = L$ and, therefore, satisfies the inequalities:

$$P_0 - L \geq \theta \geq L, \quad (19)$$

where $P_0 = P$ for the SRC with mutually prime bases, which is only inherent in R -code.

It is not difficult to make sure that the sum of any number U and the number corresponding to the error vector cannot belong to the plural L , that is, such an error can be detected. However, even in those cases when the product of the bases corresponding to erroneous symbols is greater than R , among the errors there will be those that satisfy inequalities (19) and, therefore, can be detected. The number of different errors N ($N \geq C_{\min}$) corresponding to arbitrary bases of the SRC is equal to $\Theta(N) - 1$. These errors correspond to numbers uniformly distributed in the interval $(0, P_0)$ with a step of $P_0 / \Theta(N)$. If $\Theta(N) > R$, then there will be $[\Theta(N) - 1 / R]$ errors which does not satisfy the inequality (19). The share of such errors from its total number does not exceed the value of $1 / R$. Therefore, it can be stated that the R -code allows detecting all errors of $C_{\min} - 1$ and lower multiplicity, as well as a large part of $[(R - 1) / R]$ errors of higher multiplicity.

Suppose now that a correction code with an odd minimum code distance $C_{\min}$ is used to correct errors of multiplicity w and below, where $w = (C_{\min} - 1) / 2$. Let the vector U'_1 be formed from the code word U_1 as a result of an error, the weight of which is greater than w . If the code word U_2 is found at a distance $C_{\min} \leq w$ from the vector U'_1 , then it will be accepted by the code as the correct value of the initial vector. The error could be detected if there was another code word U_3 within the distance w from the vector U'_1 . But such a situation cannot be. As, in this case, according to the property of the metric of non-positional code structures of the SRC, the code distance between U_2 and U_3 would be no more than $2w$, that is, less than the minimum code distance. Thus, to detect such an error, it is necessary that there is no code word at a distance w from the vector U'_1 . Accordingly,

if we want to correct the N -fold error, where $N > w$, then among all the vectors located at the distance $C_{\min} \leq N$ from the vector U'_1 , there should be only one code word U_1 .

In the general case, it is rather difficult to estimate the fate of errors of arbitrary weight N , which can be detected or corrected using a code with a minimum distance smaller than $C_{\min} \leq 2N + 1$. The thing is that even with fairly rough estimates, it is necessary to know not only the value of R , but also the value of each of the bases (modules) SRC (under the error modulo b_j means the distortion of the corresponding residue u_j of the number U in the SRC). For example, the fate of random errors that cannot be detected by a code that corrects N errors at a minimum code distance of $C_{\min} = 2N + 1$, can be estimated based on such considerations. Each space vector P_0 ($P_0 = P$ for the SRC with mutually prime base) can be considered a geometric point. Consider a set of spheres of radius N , the centers of which are located at points corresponding to different code words. No pair of such spheres can have common points, because otherwise the distance between the centers of such spheres would be less than the minimum code distance. Each sphere contains the same number of points X , equal to the number of different vectors with a weight that does not exceed N . It is possible to determine the value of V as the sum of all products with N or fewer bases of the SRC.

In this case, the fate of the vectors that are at a distance of $C_{\min} > N$ from the code words is determined as:

$$(P_0 - LV) / P_0 = (R - V) / R. \quad (20)$$

With arbitrary values of the error and the code word U_1 , the vector U'_1 can get to any point in space with equal probability. Therefore, it can be considered that the expression (20) determines the probability that this code will be able to detect an arbitrary error. The given estimate is not very accurate, because it does not take into account the relationship between the probability of detecting an error and the value N , which corresponds to the weight of the error itself.

To determine the probability of correcting errors of weight $N + 1$ and higher with this code, estimate (20) is not suitable, since spheres of radius $N + 1$ will necessarily have common points.

Apparently, the most realistic way to obtain information about the capabilities of each specific code is statistical modeling.

In Tables 1 and 2 show some results of such modeling for codes with a minimum code distance $C_{\min} = 3$ ($N = 1$, $\rho_1(2) \approx 0$) and $C_{\min} = 4$ ($N = 2$, $\rho(2) \approx 1$), where: $\rho_1(2)$ – the probability of correcting a double error ($N = 2$); $\rho(2)$ – the probability of the code detecting a double error ($N = 2$); $\rho(N)$ – the probability of the code detecting a N -fold error, where $N > 2$.

The SRC with bases $b_j : 3, 5, 7, 11, 13, 17, 19, 23, 29, 31$ and the common value of P (in this case, $P = P_0$ because this SRC is represented as a mutually prime base) was adopted as the initial one. Other SRCs were obtained from the initial one by eliminating

the leading bases: $P_1 = P / 31$; $P_2 = P_1 / 29$; $P_3 = P_2 / 23$; $P_4 = P_3 / 19$. For codes with a minimum code distance $C_{\min} = 3$, the degree of redundancy R was defined as the product of the two largest bases (modules), for example, for the initial SRC $R = 31 \cdot 29 = 899$; for next SRC $R_1 = 29 \cdot 23 = 667$; and for $C_{\min} = 4$ – as the product of the three largest bases (modules), for example, for the initial SRC $R = 31 \cdot 29 \cdot 23 = 20677$; for next SRC $R_1 = 29 \cdot 23 \cdot 19 = 12673$.

The value of L is equal to the product of the remaining bases (modules), but the Tables 1 and 2 does not show the value of L and R itself, but its binary logarithm, i.e., the number of bits of the equivalent binary code.

Table 1. Results of statistical modeling for codes with a minimum code distance

$$C_{\min} = 3$$

SRC	$\lceil \log_2 L \rceil$	$\lceil \log_2 R \rceil$	$\rho(2)$	$\rho(N)$
initial	25	10	0.876	0.825
1	21	10	0.868	0.810
2	18	9	0.852	0.774
3	14	9	0.852	0.768
4	10	8	0.851	0.751

Table 2. Results of statistical modeling for codes with a minimum code distance

$$C_{\min} = 4$$

SRC	$\lceil \log_2 L \rceil$	$\lceil \log_2 R \rceil$	$\rho_1(2)$	$\rho(N)$
initial	21	15	0.876	0.825
1	18	14	0.868	0.810
2	14	13	0.852	0.774
3	10	12	0.852	0.768

From the Table 2 shows that codes with a minimum code distance $C_{\min} = 4$ have a fairly high probability of correcting a double error.

In cases where the SRC represents fractions rather than integers, it is advisable to choose the interval L equal to D (for positive numbers) or $2D$ (for numbers with arbitrary signs), where D is the denominator of the fractions in the SRC, equal to the product of some bases (modules) of the SRC. Let's denote $\lambda = L / D$. In what follows, we will consider only those R -codes for which $\lambda = 1$ or $\lambda = 2$.

Let's call the bases $b_1, b_2, \dots, b_g$, the product of which is equal to D , are informational, and the remaining bases $b_{g+1}, \dots, b_k$, are control ones. Then the degree of redundancy is

equal to either the product of the control modules or half of this product. The product of control bases will be denoted by the symbol R . The connection between the number of control bases (modules) k and the minimum distance d is established by the following theorem.

Theorem 5. The number of bases (modules) R -code with a minimum code distance $C_{\min}$ cannot be less than the value $(C_{\min} - 1) + (\lambda - 1)$.

Let's prove this theorem. Let $L = D$, i.e. $\lambda - 1 = 0$. Then $R = \prod_{l=1}^k b_{g+l}$. If $k < C_{\min} - 1$, than the condition of Theorem 4 is not satisfied, since the product of $C_{\min} - 1$ SRC bases, which include k control bases, is naturally less than R .

Let's assume that $L = 2D$, i.e. $\lambda - 1 = 1$. Then $R = \frac{1}{2} \prod_{l=1}^k b_{g+l}$.

The condition of Theorem 4 can be satisfied only if $k \geq C_{\min}$ Q.E.D.

Let's present two important corollaries from this Theorem 5.

Corollary 5.1. If $\lambda = 1$ and each control base (module) is greater than any information module, then the minimum code distance is one greater than the number of control bases (modules), i.e. $C_{\min} = k + 1$.

Corollary 5.2. If $\lambda = 2$ and the product of control bases (modules) is greater than the product of any $C_{\min} - 1$ bases SRC, then the minimum code distance of the code is equal to the number of control bases (modules), i.e., $C_{\min} = k$.

So, increasing or decreasing the number of control modules, it can change the minimum distance of the code. If some SRC is expanded by adding l bases (modules), each of which is more than the bases (modules) of the initial SRC, then the minimum distance of the code is automatically increased by the amount of l . The same effect can be achieved by reducing the number of information bases (modules), i.e. moving to calculations with lower accuracy (with a smaller denominator of fractions). Consequently, there is an inversely proportional relationship between the correcting capabilities of the codes and the calculated accuracy. On one and the same IPS, it is possible to perform some calculations with high accuracy, but low reliability, and others with less accuracy, but with higher reliability and speed, since the execution time of basic operations is proportional to the number of information bases (modules) [44].

From the nature of the considered SRC correction codes, its complete arithmetic nature is visible – the entered bases are included in the general system of the SRC bases and codes containing numbers for all both information and control bits are involved in any operation of the control information and control system; the processing of the main and additional digits is done in exactly the same way, without any difference [43]. This allows us to assume that information processing in the SRC can be carried out without monitoring each intermediate result obtained. The size (length) of the control stage is determined in each individual case either by a completed cycle of processing an array of information, or

in accordance with the probability of a single error occurring. The final result of the calculations of each stage may be subject to control and its correctness confirms the correctness of all operations at this stage [45]. Note that the introduction of only one control base makes it possible to detect not only any single error, as in the positional numeral system, but also most double errors.

Currently, the possibilities of non-linear codes (*R*-codes) for error correction in the SRC are being intensively researched. This is due to the simplicity of the *R*-code structure and good corrective capabilities, as well as the comparative ease of its construction for any given minimum code distance.

CHAPTER 5. DEVELOPMENT OF A METHOD FOR DETECTING AND CORRECTING ERRORS IN THE SRC BASED ON THE USE OF L -CODES

It should be noted that to date, an in-depth study of the properties of the SRC, the bases of which are mutually pairwise non-prime numbers, has not been carried out. It is natural to assume that such a system also has certain corrective properties, which necessitates an assessment of the possibility and feasibility of using such systems to increase the reliability of the IPS.

It is important and interesting to consider the so-called linear codes (L -codes) in the SRC. In the literature, L -codes are described qualitatively rather than quantitatively. The fact is that until now no one has been engaged in a deep study of the properties of systems of residual classes, the bases of which are mutually prime numbers. Such a system also has certain corrective properties, which makes it necessary to assess the possibility and expediency of using such systems to increase the reliability of the IPS [46].

At the same time, apart from the above-mentioned advantage of L -codes in the simplicity of the decoding operation of non-positional code structures (technical simplicity of the decoding device), L -codes have another important advantage, namely the high speed of the operation of detecting and correcting errors in the code word in comparison with R -codes codes.

It is known that the sum, difference and product of any vectors of a linear L -code are code words. In this case, no natural numbers can be assigned to non-code words. Let's show that error correction in SRC using linear codes leads to hardware redundancy equivalent to redundancy.

According to Theorem 3, the minimum code distance $C_{\min}$ of a correcting linear L -code in the SRC is equal to the minimum weight of non-zero code words. It follows from the Theorem 3 that the minimum code distance $C_{\min}$ can be determined if the weights of the code words are known. We will also additionally present one more theorem, which more widely reveals the features of the L -code in the SRC.

Theorem 6. In order for L -code to have a minimum distance $C_{\min}$, it is necessary and sufficient that the degree of redundancy R satisfies the relation $R = P^{C_{\min}-1}$.

From Theorem 6 it follows that the correction of arbitrary information errors in the SRC using L -codes leads to large redundancy, equivalent to redundancy.

Thus, it is ineffective to use L -codes for error corrections, which with equal probability correspond to arbitrary distortions of the residue of the code words in the SRC. However, if you limit the class of possible errors in individual residues of code words, the capabilities of L -codes expand significantly [46]. To determine the necessary and sufficient conditions for detecting one-time errors using A -codes, based on Lemma 4.1, the following theorem is formulated and proven.

Lemma 6.1. For any integer $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ in the SRC with bases $b_j (j = \overline{1, g})$ and for any pair of bases b_j and b_q , the condition $u_j - u_q \equiv 0 \pmod{d_{jq}}$ must be satisfied, where d_{jq} is the greatest common divisor of the bases b_j and b_q , $j, q = \overline{1, g}; j \neq q$.

To determine the necessary and sufficient conditions for detecting one-time errors using L -codes, based on Lemma 6.1, the following theorem is formulated and proven.

Theorem 7. To detect errors in the residue of an arbitrary base $b_j (j = \overline{1, g})$ of a number $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ specified in the SRC with bases $b_1, \dots, b_g$, it is necessary that the base b_j has at least one common divisor d_{jq} other than one with the other bases $b_j (j \neq q)$.

Proof. Let the greatest common divisor $d_{jq}(b_j, b_q)$ be defined for arbitrary bases SRC ($j \neq q$), and the error occurred at the base b_j , i.e. the distorted residue $\tilde{u}_j = u_j + \theta$ is appeared. Let's show that the expression $\tilde{u}_j - u_j$ is equivalent to $\theta \pmod{d_{jq}}$, i.e. $\tilde{u}_j - u_j = \theta \pmod{d_{jq}}$.

According to the Lemma 6.1, the following equality is satisfied: $u_j - u_q = 0 \pmod{d_{jq}}$.

Let's write the expression $u_j + \theta = \tilde{u}_j \pmod{b_j}$ in the form $u_j + \theta = m \cdot b_j \cdot \tilde{u}_j$, where m is an integer; $b_j = k \cdot d_{jq}$, where k is a natural number. From the last expression we determine the distorted residue $\tilde{u}_j = u_j + \theta - m \cdot b_j$. Then it can be written $\tilde{u}_j - u_j = [(u_j - u_q) + (-m \cdot k \cdot d_{jq}) + \theta]$.

Since $u_j - u_q \equiv 0 \pmod{d_{jq}}$ and $-m \cdot k \cdot d_{jq} = 0 \pmod{d_{jq}}$, then $\tilde{u}_j - u_j \equiv \theta \pmod{d_{jq}}$.

It is obvious that in the absence of common divisors $\theta \equiv 0 \pmod{d_{jq}}$, i.e. if $d_{jq} = 1$, which proves the necessary condition of the Theorem 7.

The necessary condition of the Theorem 7 is sufficient if the error is not a multiple of the divisor d_{jq} . Really, $m \cdot d_{jq} + u_{jq} \neq 0 \pmod{d_{jq}}$, where $u_{jq} = u_j - u_q$, for $0 < u_{jq} < d_{jq}$.

Theorem 7 can also be formulated as follows.

To detect an error in the residue to an arbitrary base b_j of the number $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ specified in the SRC, it is necessary and sufficient that the error θ is not a multiple of the divisors d_{jq} and d_j , where $d_j = (d_{j1} \parallel d_{j2} \parallel \dots \parallel d_{jg})$ is the greatest common divisor of the divisors $d_{j1}, d_{j2}, \dots, d_{jg}$.

At the moment, there are many algorithms and methods for detecting errors in the SRC with mutually pairwise simple bases; there are no detection methods for other types of bases. Thus, it is possible to propose a procedure for detecting errors in the SRC with mutually pairwise non-prime bases and create an algorithm that implements it.

The developed algorithm for detecting errors in the SRC with mutually pairwise non-prime bases consists of the following actions:

1. The residue is checked by base b_j . To do this, we define a set of values:

$$u_1 - u_2 = u_{12} \bmod d_{12},$$

$$u_1 - u_3 = u_{13} \bmod d_{13},$$

$$u_1 - u_g = u_{1g} \bmod d_{1g}.$$

If $u_1 - u_j = 0 \bmod d_{1j}$, then the second residue is checked, etc.

2. To obtain the values of u_{jq} ($j \neq q$), a matrix is compiled:

$$M = \begin{bmatrix} u_{12} & u_{13} & \dots & u_{1g} \\ u_{21} & u_{23} & \dots & u_{2g} \\ \vdots & & & \\ u_{n1} & u_{n2} & \dots & u_{g-1g} \end{bmatrix}.$$

When compiling matrix M , it is not necessary to indicate the true numerical value of u_{jq} ; it is enough to present its distinctive feature:

$$u_{jq} = \begin{cases} 0, & \text{if } u_j - u_q = 0 \bmod d_{jq}, \\ 1, & \text{if } u_j - u_q \neq 0 \bmod d_{jq}. \end{cases}$$

3. If the determinant $|M|$ of the matrix is zero, then the number $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ is correct, and if $|M| \neq 0$, then the number U is incorrect.

Let's consider considerations that allow us to simplify the above algorithm.

Based on the fact that $u_j - u_q \equiv [d_{jq} - (u_j - u_q)] \bmod d_{iq}$, the determinant $|M|$ cannot be sought. It is enough to determine the diagonal elements of the M matrix and add one value of u_{g1} , i.e. $u_{12}, u_{23}, u_{34}, \dots, u_{g-1g}, u_{g1}$.

It is easy to check that for such values of u_{jq} , it is possible to establish as a fact the distorted code word, and also to determine the number of the distorted residue.

In order to determine the necessary and sufficient conditions for correcting one-time errors using L -codes, the following theorem was formulated and proved.

Theorem 8. To correct an error in the residue by an arbitrary base b_j of the number $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ given in the SRC with bases $b_1, b_2, \dots, b_g$, the condition must be fulfilled:

$$(d_{jk} - 1)(d_{jq} - 1) \geq b_i - 1 - \left(N_{d_{jk}} + N_{d_{jq}} - N_{[d_{jk}, d_{jq}]} \right), \quad (21)$$

where d_{jk} is the greatest common divisor of the bases b_j and b_k ;

d_{jq} is the greatest common divisor of the bases b_j and b_q ;

$N_{d_{jk}}$ is the number of divisors that are multiples of d_{jk} ;

$N_{[d_{jk}, d_{jq}]}$ is the number of divisors that are multiples of the lowest common multiple $[d_{jk}, d_{jq}]$ of the divisors of d_{jk} and d_{jq} ($j \neq q, k \neq q$).

Proof. Let's calculate the value of u_{jq}, u_{jk}, u_{qk} . If the error occurred by base of b_j , then $u_{qk} = 0, u_{jq} \neq 0$ and $u_{jk} \neq 0$. The number of different combinations u_{jq}, u_{jk} is equal to $(d_{jq} - 1) \cdot (d_{jk} - 1)$, where $(d_{jq} - 1)$ is the number of possible values of u_{jq} ($u_{jq} \neq 0$); $(d_{jk} - 1)$ – the number of possible values of u_{jk} ($u_{jk} \neq 0$), and the number of possible error values by based b_j is equal to $b_j - 1$ ($\theta \neq 0$), minus the number of undetected errors. The number of undetected errors consists of the number of errors multiples of the divisor $d_{jk} - N_{d_{jk}}$ and multiples of the divisor $d_{jq} - N_{d_{jq}}$. Thus, the number of possible error values detected is equal to $b_j - 1 - (N_{d_{jk}} + N_{d_{jq}} - N_{[d_{jk}, d_{jq}]})$.

To ensure compliance with the possible values of errors by base b_j , the following inequality must be satisfied:

$$(d_{jq} - 1)(d_{jk} - 1) \geq b_j - 1 - (N_{d_{jk}} + N_{d_{jq}} - N_{[d_{jk}, d_{jq}]}).$$

What needed to be proven.

The necessary condition of Theorem 8 is sufficient if different values of the errors θ correspond to different values of the product $u_{jk} \cdot u_{jq}$ and vice versa. Indeed, in this case, there is a mutually unambiguous correspondence between the possible values of θ and the values of the product $u_{jk} \cdot u_{jq}$, which determines the possibility of unambiguously determining the magnitude of the error. In other words, the necessary condition of Theorem 8 is sufficient if the error $\theta = \tilde{u}_j - u_j$ not divisible by divisors d_{j-1j}, d_{jj+1} , i.e. by next two divisors $d_{\theta}^{(j-1)} = (d_{j-1j}, \theta) = 1, d_{\theta}^{(j+1)} = (d_{jj+1}, \theta) = 1$.

On the basis of Theorem 8, we obtain a procedure for correcting errors for an arbitrary base and create an algorithm that implements it:

1. Let's determine the number of the distorted residue. For this purpose the values are calculated:

$$\begin{aligned} u_1 - u_2 &= u_{12} \bmod d_{12}, \\ u_2 - u_3 &= u_{23} \bmod d_{23}, \\ &\dots \\ u_{g-1} - u_g &= u_{g-1g} \bmod d_{g-1g}, \\ u_g - u_1 &= u_{g1} \bmod d_{g1}. \end{aligned}$$

If all residues are $u_{jq} = 0 \pmod{d_{jq}}$, then the number $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ is correct, or the error is a multiple of each of the divisors d_{j-1j}, d_{jj+1} , (a single error is assumed). If

the error occurred by an arbitrary base b_j , then $u_{jq} \neq 0$ and $u_{jk} \neq 0$, and all other values are $u_{kg} = 0$. Thus, the number $\tilde{U} = (u_1 \parallel u_2 \parallel \dots \parallel \tilde{u}_j \parallel \dots \parallel u_g)$ being tested is incorrect.

2. The values of u_{jq} and u_{jk} are followed by a block of error constants, where the corresponding values of θ are collected.

3. Let's correct the number $\tilde{U}$ in the residue u_j and get the correct number $U = \tilde{U} - \theta$, i.e. $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$.

If in the abbreviated SRC, due to the exclusion of the base on which the error occurred, it is possible to clearly imagine the number U , then instead of determining the error value by the values of u_{jq} and u_{jk} , we directly calculate the value of the correct residue u_j .

Consider this error correction algorithm:

1. Let's calculate the values of the residuals $u_{12}, u_{23}, \dots, u_{g1}$.

2. Determine the number of the distorted residue. Let the error occur by the base b_j . In this case, this base is excluded, and the number U is represented on the bases $b_1, b_2, \dots, b_{j-1}, b_{j+1}, \dots, b_g$, i.e.:

3. The number U is convolved into a positional code.

4. The true value of the distorted residue $u_j = U - [U / b_j] b_j$, is determined, where $[x]$ is the whole part of x , not exceeding x . Then the corrected number is $U_{cor} = (u_1 \parallel u_2 \parallel \dots \parallel u_j \parallel \dots \parallel u_g)$.

We will determine the conditions under which it is possible to exclude some bases from the SRC. To do this, we will present the bases of the original SRC in the canonical form:

$$b_1 = \beta_{11}^{i_{11}} \cdot \beta_{12}^{i_{12}} \cdot \dots \cdot \beta_{1l_1}^{i_{1l_1}},$$

$$b_2 = \beta_{21}^{i_{21}} \cdot \beta_{22}^{i_{22}} \cdot \dots \cdot \beta_{2l_2}^{i_{2l_2}},$$

...

$$b_g = \beta_{g1}^{i_{g1}} \cdot \beta_{g2}^{i_{g2}} \cdot \dots \cdot \beta_{gl_g}^{i_{gl_g}},$$

$$P = \beta_1^{i_1} \cdot \beta_2^{i_2} \cdot \dots \cdot \beta_k^{i_k}.$$

To unambiguously determine the number U given in the SRC with bases $b_1, b_2, \dots, b_g$ and lying in the range of $[0, P)$, it is possible to exclude only those bases for which $\beta_s = \beta_{jl_j} (s = \overline{1, k}; j = \overline{1, g})$. In this case, it is necessary that $i_s \geq i_{jl_j}$.

Thus, the necessary and sufficient conditions for error correction by the method of excluding the distorted base have been determined. These conditions are the simultaneous fulfillment of equality and inequality:

$$\beta_s = \beta_{j_l}; i_s \geq i_{j_l}. \quad (22)$$

Let the SRC be given by bases $b_1 = 4$, $b_2 = 6$, $b_3 = 12$, $b_4 = 18$. At the same time, the use of L -codes assumes that the SRC is represented by mutually pairwise non-prime bases, which implies that the range of representation of P code words will be determined as the least common multiple (LCM) of all the bases of this SRC, i.e. least common multiple $P = LCM[4, 6, 12, 18] = 36$. In accordance with the condition for the possibility of error correction (22), we will determine those bases of the SRC that can be excluded. Let's present the bases of the SRC in the canonical form: $b_1 = 2^2$, $b_2 = 2 \cdot 3$, $b_3 = 2^2 \cdot 3$, $b_4 = 2 \cdot 3^2$ and $P = 2^2 \cdot 3^2 = 36$. It is obvious that the sought bases are b_1, b_2, b_3 . We will carry out a check, for this we will find the partial values of the LCM: $P_1 = LCM[6, 12, 18] = 36$, $P_2 = LCM[4, 12, 18] = 36$, $P_3 = LCM[4, 6, 18] = 36$, $P_4 = LCM[4, 6, 12] = 24$.

The value of LCM $P_4 = 24 < 36$, which confirms the correctness of the determination of the bases that are excluded from the given SRC.

According to the proposed algorithm for detecting and correcting errors in the SRC using L -codes, we will consider the procedure for detecting and correcting errors.

Suppose that when calculating the values of $(u_k - u_{k+1}) \bmod d_{kk+1}$ it is determined that $u_{j-1j} \neq 0$, $u_{jj+1} \neq 0$ and all other values are equal to $u_{kk+1} = (u_k - u_{k+1}) \bmod d_{kk+1} = 0$.

Then it is claimed that the number U is incorrect, and the error is in the residue by base b_j , i.e. $\tilde{U} = (u_1 \parallel u_2 \parallel \dots \parallel \tilde{u}_{j-1} \parallel \tilde{u}_j \parallel \tilde{u}_{j+1} \parallel \dots \parallel u_g)$.

Referring to the values of u_{j-1j} and u_{jj+1} to the block of error constants, we determine the error value θ_j and then determine the true value of the residue $u_{j\text{ cor}} = \tilde{u}_j - \theta_j$, where θ_j – error that occurred in the residue u_j .

The corrected number will be presented in the form: $U_{\text{cor}} = (u_1 \parallel u_2 \parallel \dots \parallel u_{j\text{ cor}} \parallel \dots \parallel u_g)$.

To correct an error using the developed method, it is necessary that the error θ_j is simultaneously not a multiple of two divisors d_{j-1j} and d_{jj+1} which limits the class of errors being corrected.

Thus, there is a need to develop effective procedures and algorithms to expand the class of possible correctable errors.

The procedure for correcting single errors, which allows us to correct errors that are non-multiples of one of the divisors d_{j-1j} and d_{jj+1} , is as follows.

Let SRC with mutually non-prime bases be given, i.e. greatest common divisor $(b_1, b_2, \dots, b_g) \geq 2$. And let the number in the SRC $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ be given.

Let's determine all the values of u_{kk+1} , i.e. $u_{12}, u_{23}, u_{34}, \dots, u_{g-1g}, u_{g1}$. Without violating the commonality of reasoning, we will assume that $u_{jj+1} \neq 0$ and all other values of $u_{kk+1} = 0$.

Since $u_{jj+1} = (u_j - u_{j+1}) \bmod d_{jj+1} \neq 0$, the error can only be in the residue by bases b_j or b_{j+1} . In this regard, two hypotheses are possible:

- an error is present in the residue u_j ;
- an error is present in the residue u_{j+1} .

Before considering the process of error correction by the proposed method, we will formulate and prove a Theorem 9, the result of the proof of which we use for the process of convergence of a set of numbers of the form: $U^{(kj)} = (u_1 \parallel \dots \parallel u_{i-1} \parallel u_{jkj} \parallel u_{i+1} \parallel \dots \parallel u_g)$ to the correct number $U^{(\varphi)} = (u_1 \parallel \dots \parallel u_{i-1} \parallel u_{j\varphi} \parallel u_{j+1} \parallel \dots \parallel u_g)$.

Before considering Theorem 9, we first consider the lemma for this theorem.

Lemma 9.1. The sum, difference, and product of any L -code code words are code words.

Theorem 9. Let an incorrect (distorted in one residue) number $\tilde{U} = (u_1 \parallel u_2 \parallel \dots \parallel \tilde{u}_{j-1} \parallel \tilde{u}_j \parallel \tilde{u}_{j+1} \parallel \dots \parallel u_g)$ be given in the ordered $(b_{j-1} < b_j; j = \overline{1, g})$ SRC with bases $b_1, \dots, b_g$ and let $\theta_j = \tilde{u}_j - u_j = k_j \cdot d_{j-1j}$.

Then in the set of values of $u_{jk_j} = (\tilde{u}_j - k_j \cdot d_{j-1j}) \bmod b_j$ there is such a single value of $u_{j\varphi}$ in which the number $U^{(\varphi)} = (u_1 \parallel \dots \parallel u_{i-1} \parallel u_{j\varphi} \parallel u_{j+1} \parallel \dots \parallel u_g)$ is a correct number, where d_{j-1j} is the greatest common divisor of the bases b_{j-1} and b_j ; and k_j can take the value of $k_j = 1, 2, \dots, b_j / d_{j-1j} - 1$.

Proof. Let's show that there exists such a value of $u_{j\varphi_1}$ for which the number $U^{(\varphi_1)} = (u_1 \parallel \dots \parallel u_{j\varphi_1} \parallel \dots \parallel u_g)$ is correct. According to the condition of the Theorem 9, the error θ_j is a multiple of the divisor d_{j-1j} . The expression $k_j \cdot d_{j-1j}$ contains all possible multiples of $1 \cdot d_{j-1j}$. Thus, there will be at least one value of $k_j = \varphi_1$ for which $\theta_{j\varphi_1} = \varphi_1 \cdot d_{j-1j}$ and $u_{j\varphi_1} = \tilde{u}_j - \theta_{j\varphi_1} = \tilde{u}_j - \varphi_1 \cdot d_{j-1j}$.

Let's show that $U^{(\varphi_1)}$ is the only correct number from the set of numbers of the form $U^{(k_j)}$.

Suppose that there is such a value of $u_{j\varphi_2} = \tilde{u}_j - \varphi_2 \cdot d_{j-1j}$, at which the number $U^{(\varphi_2)}$ is also correct. Then, according to Lemma 9.1, the number $U^{(\varphi_1)} - U^{(\varphi_2)} = (0 \parallel \dots \parallel u_{j\varphi_1} - u_{j\varphi_2} \parallel \dots \parallel 0)$ is correct. If the number $U^{(\varphi_1)} - U^{(\varphi_2)}$ is correct, then according to Lemma 6.1 we have:

$$(\varphi_2 - \varphi_1)d_{j-1j} \equiv 0 \bmod d_{j-1j},$$

$$(\varphi_2 - \varphi_1)d_{j-1j} \equiv 0 \pmod{d_{2-j}},$$

...

$$(\varphi_2 - \varphi_1)d_{j-1j} \equiv 0 \pmod{d_{g-j}}.$$

If $j \neq g$, then the only correct number $U^{(\varphi_1)} - U^{(\varphi_2)}$ will be a zero code word. This is due to the fact that $d_{j-1j} \neq 0$ and d_{j-1j} are not equal to the least common multiple of the divisors of $d_{1j}, d_{2j}, \dots, d_{gj}$. Moreover, the inequality $d_{j-1j} \neq [d_{1j}, d_{2j}, \dots, d_{gj}]$ contradicts the condition of arbitrary choice of bases of $b_1, b_2, \dots, b_g$. Therefore, the following equality $U^{(\varphi_1)} - U^{(\varphi_2)} = (0 \parallel 0 \parallel \dots \parallel 0 \parallel \dots \parallel 0)$ is fulfilled.

Thus, $\varphi_1 = \varphi_2$, which confirms the uniqueness of the existence of φ_1 for which $U^{(\varphi_1)} = (u_1 \parallel \dots \parallel u_{j\varphi_1} \parallel \dots \parallel u_g)$ is correct. What needed to be proven.

Let's develop an error correction algorithm based on the result of the proven Theorem 9.

Let's consider the first hypothesis. Since $u_{j-1j} = 0$, then the error is a multiple of the divisor d_{j-1j} . Therefore, the error by base can take the value for $\theta_j = k \cdot d_{j-1j}$, for $k = 1, 2, \dots, b_j / d_{j-1j} - 1$.

Let's calculate the set of values $u_{jk_j} = (u_j - k_j \cdot d_{j-1j}) \pmod{b_j}$.

If in this population there is a value of u_{js} , for which $U^{(s)} = (u_1 \parallel u_2 \parallel \dots \parallel u_{js} \parallel \dots \parallel u_g)$ is a correct number, the first hypothesis is valid, that is, an error is present in the residue by base b_j .

In this case, the corrected number is $U_{cor} = U^{(s)}$, where $u_{js} = (u_j - k \cdot d_{j-1j}) \pmod{b_j}$.

If for all values of u_{jk_j} , the number $U^{(k_j)}$ is incorrect, then the value of u_j is true, and the error occurred in the residue by base b_{j+1} . Since $u_{j+1j+2} = 0$, the error by base b_{j+1} is a multiple of the divisor d_{j+1j+2} , i.e. $\theta_{j+1} = k_{j+1} \cdot d_{j+1j+2}$, where $k_{j+1} = 1, 2, \dots, b_{j+1} / d_{j+1j+2} - 1$.

Let's define a set of values:

$$u_{j+1k_{j+1}} = (u_{j+1} - k_{j+1} \cdot d_{j+1j+2}) \pmod{b_{j+1}}$$

According to Theorem 9, in this set there must be such a single number u_{j+1N} , for which $U^{(N)} = (u_1 \parallel u_2 \parallel \dots \parallel u_{j+1N} \parallel \dots \parallel u_g)$ is a correct number.

Note that the sequence of hypothesis testing is arbitrary and does not affect the probability of error correction.

However, in order to increase the speed of determining the number of the distorted residue, it is first necessary to check the hypothesis for which the value of b_k / d_{k-1k} ($k = j, j+1$) will be the smallest.

Consider an example of the implementation of the developed error correction algorithm using L -codes.

Let the SRC be given by the bases $b_1 = 4$, $b_2 = 6$, $b_3 = 12$, $b_4 = 18$. At the same time, $L = P = LCM[4, 6, 12, 18] = 36$, $d_{12} = 2$, $d_{23} = 6$, $d_{34} = 6$, $d_{41} = 2$. The volume of code words is presented in the Table. 3.

It is necessary to determine the correctness of the number $U = (3 \parallel 5 \parallel 7 \parallel 7)$ and, in case of distortion, correct it.

1. Determine the value of $u_{12} = 0$, $u_{23} = 2$, $u_{34} = 0$, $u_{41} = 0$. Since $u_{23} \neq 0$, the number U is incorrect, and the error occurred in the second or third residue.

2. Since $b_2 / d_{12} > b_3 / d_{34}$, the first hypothesis is that the error is assumed in the residue by base b_3 .

3. Let's calculate the value of $u_{3k_3} = u_3 - k_3 \cdot d_{23}$ for $k_3 = 1$.

Let's get $u_{3k_3} = u_3 - k_3 \cdot d_{23} = 7 - 1 \cdot 6 = 1$. At the same time, the received number $U^{(1)} = (3 \parallel 5 \parallel 1 \parallel 7)$ is not a code word (see Table. 3), that is, the first hypothesis is not true. An error occurred in the residue by base b_2 .

4. Let's correct the number $U = (3 \parallel 5 \parallel 7 \parallel 7)$. To do this, we will determine the desired value of $k_2 = 1; 2$ from the values of $u_{2k_2} = u_2 - k_2 \cdot d_{21}$:

$$k_2 = 1, \quad u_{2k_2} = u_2 - k_2 \cdot d_{21} = 5 - 1 \cdot 2 = 3,$$

$$k_2 = 2, \quad u_{2k_2} = u_2 - k_2 \cdot d_{21} = 5 - 2 \cdot 2 = 1.$$

Table 3. Table of code words

Number U in decimal code	Number U in the SRC			
	$b_1 = 4$	$b_2 = 6$	$b_3 = 12$	$b_4 = 18$
0	0	0	0	0
1	1	1	1	1
2	2	2	2	2
3	3	3	3	3
4	0	4	4	4
5	1	5	5	5
6	2	0	6	6
7	3	1	7	7
8	0	2	8	8
9	1	3	9	9
10	2	4	10	10
11	3	5	11	11
12	0	0	0	12
13	1	1	1	13
14	2	2	2	14
15	3	3	3	15
16	0	4	4	16
17	1	5	5	17
18	2	0	6	0
19	3	1	7	1
20	0	2	8	2
21	1	3	9	3
22	2	4	10	4
23	3	5	11	5
24	0	0	0	6
25	1	1	1	7
26	2	2	2	8
27	3	3	3	9
28	0	4	4	10
29	1	5	5	11
30	2	0	6	12
31	3	1	7	13
32	0	2	8	14
33	1	3	9	15
34	2	4	10	16
35	3	5	11	17

In this way, we will get two code words: $U^{(1)} = (3 \parallel 3 \parallel 7 \parallel 7)$ and $U^{(2)} = (3 \parallel 1 \parallel 7 \parallel 7)$. Table 3 shows that the only correct code word is the value $U^{(2)} = (3 \parallel 1 \parallel 7 \parallel 7)$, i.e. $U_{cor} = U^{(2)} = (3 \parallel 1 \parallel 7 \parallel 7)$.

Thus, the developed method of error correction in the SRC allows to expand the class of corrected errors. This significantly expands the corrective capabilities of L -codes in the class of deductions. Consider the operation of the device for detecting errors using L -codes, according to the algorithm discussed above. This device contains an input register, modulo adders b_j , d_{1j} ($j = \overline{2, g}$) and $(g-1)$ is the OR input element (see Fig. 1). The operation algorithm of this device corresponds to the error detection algorithm developed above.

Let SRC be given by bases $b_1 = 4$, $b_2 = 6$, $b_3 = 12$. With $\prod_{j=1}^3 b_j = 288$, $L = P = LCM[4, 6, 12] = 12$, $d_{12} = (4, 6) = 2$, $d_{13} = (4, 12) = 4$.

Let's determine the correctness of the number $U = (11 \parallel 001 \parallel 0111)$.

At the output of the adder modulo b_2 , we will get $\bar{u}_2 = b_2 - u_2 = 0101$, at the output of the adder modulo b_3 : $\bar{u}_3 = b_3 - u_3 = 0101$.

At the output of the adder modulo d_{12} , we get $u_1 + \bar{u}_2 = 0 \bmod d_{12}$, at the output of the adder d_{13} : $u_1 + \bar{u}_3 = 0 \bmod d_{13}$.

There is no signal at the output of the device, that is, the number is correct (see Table 4).

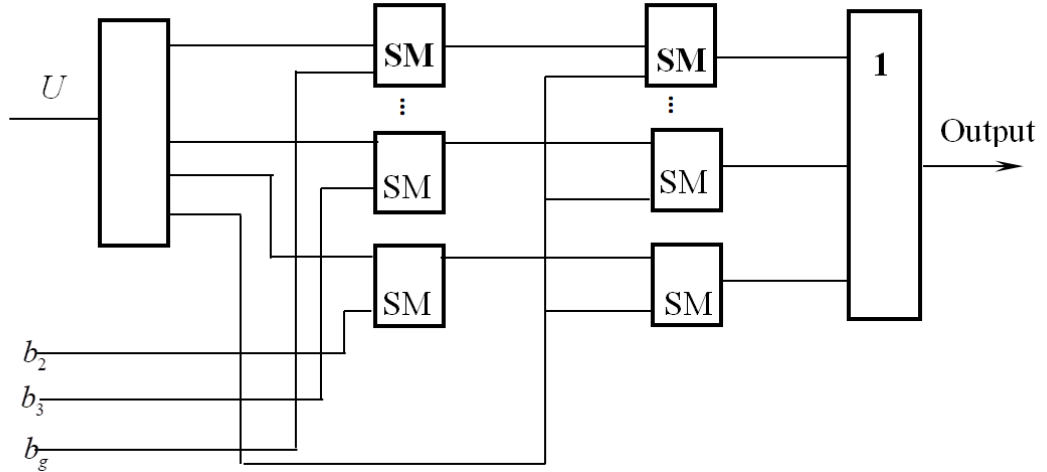


Figure 1. A device for detecting errors in the SRC

Table 4. Table of code words

U_j	Code numbers U in the SRC		
	$b_1 = 4$	$b_2 = 6$	$b_3 = 12$
0000	00	000	0000
0001	01	001	0001
0010	10	010	0010
0011	11	011	0011
0100	00	100	0100
0101	01	101	0101
0110	10	000	0110
0111	11	001	0111
1000	00	010	1000
1001	01	011	1001
1010	10	100	1010
0101	11	101	1011

Let the number U be distorted based on b_2 and let $\theta_2 = 011$, i.e.: $\tilde{U} = (0011 \parallel 0100 \parallel 0111)$. At the output of the adder modulo b_2 we will get a number: $\bar{u}_2 = b_2 - \tilde{u}_2 = 010$. And at the output of the adder modulo b_3 is a number $\bar{u}_3 = b_3 - u_3 = 0101$.

At the output of the adder modulo d_{12} we will get $u_1 + \bar{u}_2 = 1 \bmod d_{12}$, and modulo d_{13} : $u_1 + \bar{u}_3 = 0 \bmod d_{13}$. At the output of the device, we will receive the operand 0001, that is, the number is incorrect.

As can be seen from the considered examples of the specific implementation of the error correction operation, the process of error detection is simply implemented with the help of L -codes.

The error detection time for the SRC given by any bases system is always equal to three conditional time clocks and does not depend (as it is observed for R -codes) on the number n of information bases.

Let's give some considerations that will simplify the above device Fig. 1 and create a more schematically simple device for detecting errors (Fig. 2).

First, we will prove the ratio $u_1 + \bar{u}_j = (\bar{u}_1 + u_j) \bmod d_{1j}$, on the basis of which we will compile an error correction algorithm. On the basis of which we will compile an error correction algorithm. Let the number $U = (u_1 \parallel u_2 \parallel \dots \parallel u_g)$ have the distorted residue by base b_q , i.e. $\tilde{u}_q = (u_q + \theta_q) \bmod b_q$.

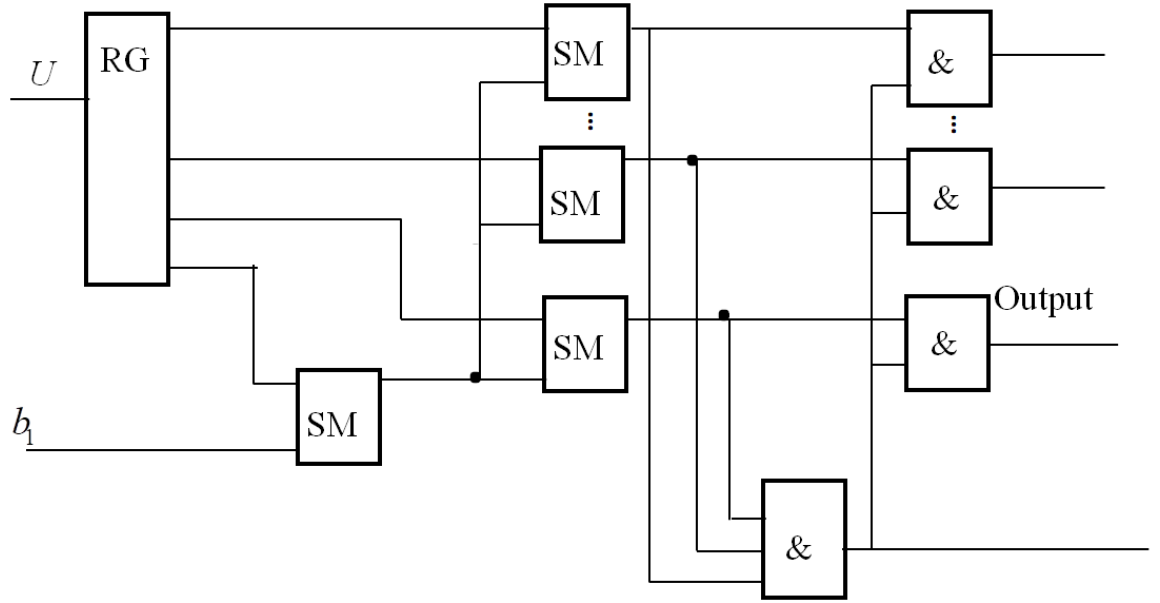


Figure 2. A simplified device for detecting errors in the SRC

Let's write down the system of equalities:

$$k_1 = u_j - \tilde{u}_q = u_j + (b_q - \tilde{u}_q) = (u_j - u_q + b_q - \theta_q) \bmod b_q,$$

$$k_2 = \tilde{u}_q - u_j = u_q + \theta_q - u_j = (u_q - u_j + u_q) \bmod b_q.$$

Let's add these equalities and get $k_1 + k_2 = b_q \pmod{b_q}$ or $k_1 + k_2 = 0 \pmod{d_{jq}}$.

Thus, it is shown that $u_1 + \bar{u}_j = (\bar{u}_1 + u_j) \bmod d_{1j}$, i.e. in the device for detecting errors instead of $g - 1$ adders modulo b_j , it is enough to have only one adder modulo b_1 .

The developed algorithm for the implementation of the error detection process is determined by the following ratios:

$$u_2 + b_1 - u_1 = (u_2 + \bar{u}_1) \bmod d_{12},$$

$$u_3 + b_1 - u_1 = (u_3 + \bar{u}_1) \bmod d_{13}.$$

The above-considered variants of devices for determining errors in the SRC make it possible to reliably detect the fact of distortion of the number U , however, at the same time, the number of the base on which the distortion of the residue occurred is not determined.

Consider a device that determines the number of the residue by which the number U distortion occurred.

Let the SRC be given by the bases $b_1 = 4$, $b_2 = 6$, $b_3 = 12$, $b_4 = 18$. At the same time, $L = P = LCM[4, 6, 12, 18] = 36$, $d_{12} = (4, 6) = 2$, $d_{23} = (6, 12) = 6$, $d_{34} = (12, 18) = 6$, $d_{41} = (18, 4) = 2$, $U = (0 \parallel 2 \parallel 8 \parallel 2)$.

Let the number U be distorted in the residue by base b_4 , that is $\bar{u}_2 = b_2 - u_2 = 4$ and let $\theta_4 = 5$.

At the output of the adder modulo b_2 we get the value of $\bar{u}_2 = b_2 - u_2 = 4$, modulo b_3 we get $\bar{u}_3 = b_3 - u_3 = 4$, at the output of the adder modulo b_4 : $\bar{u}_4 = b_4 - u_4 = 11$. At the output of the adder modulo d_{12} we get $u_1 + \bar{u}_2 = 0 \bmod d_{12}$; modulo d_{23} : $u_2 + \bar{u}_3 = 0 \bmod d_{23}$; modulo d_{34} : $u_3 + \bar{u}_4 = 1 \bmod d_{34}$; modulo d_{41} : $u_4 + \bar{u}_1 = 1 \bmod d_{41}$.

At the inputs of adders modulo d_{34} and d_{41} there is a non-zero result of operation $(u_s + \bar{u}_q) \bmod d_{sq}$, so the fourth element AND (&) is open, that is, there is a signal on the fourth output bus. It follows that the error occurred in the fourth residue u_4 (see Table 5).

Based on the proven Theorem 8, condition (21) is a necessary condition for detecting an error in the remainder modulo b_j . This condition is also sufficient if the error $\theta_j = \tilde{u}_j - u_j$ is not a multiple of the divisors d_{j-1j} and d_{jj+1} at the same time, that is, the next two divisors $d_{\theta_j}^{(j-1)} = (d_{j-1j}, \theta_j) = 1$, $d_{\theta_j}^{(j+1)} = (d_{jj+1}, \theta_j) = 1$.

Table 5. Table of code words for the set of the SRC bases

Num ber U in deci- mal code	Code words in the SRC				Num ber U in deci- mal code	Code words in the SRC			
	$b_1 = 4$	$b_2 = 6$	$b_3 = 12$	$b_4 = 18$		$b_1 = 4$	$b_2 = 6$	$b_3 = 12$	$b_4 = 18$
0	0	0	0	0	18	2	0	6	0
1	1	1	1	1	19	3	1	7	1
2	2	2	2	2	20	0	2	8	2
3	3	3	3	3	21	1	3	9	3
4	0	4	4	4	22	2	4	10	4
5	1	5	5	5	23	3	5	11	5
6	2	0	6	6	24	0	0	0	6
7	3	1	7	7	25	1	1	1	7
8	0	2	8	8	26	2	2	2	8
9	1	3	9	9	27	3	3	3	9
10	2	4	10	10	28	0	4	4	10
11	3	5	11	11	29	1	5	5	11
12	0	0	0	12	30	2	0	6	12
13	1	1	1	13	31	3	1	7	13
14	2	2	2	14	32	0	2	8	14
15	3	3	3	15	33	1	3	9	15
16	0	4	4	16	34	2	4	10	16
17	1	5	5	17	35	3	5	11	17

According to the results of Theorem 8, we will construct an error correction algorithm from an arbitrary base b_j :

1. Let's define all possible values of the type $u_j - u_{j+1} = u_{j \ j+1} \bmod d_{j \ j+1}$:

$$\begin{cases} u_1 - u_2 = u_{12} \bmod d_{12}, \\ u_2 - u_3 = u_{23} \bmod d_{23}, \\ \dots \\ u_{g-1} - u_g = u_{g-1 \ g} \bmod d_{g-1 \ g}, \\ u_g - u_1 = u_{g1} \bmod d_{g1}. \end{cases} \quad (23)$$

2. If all values (23) are equal to zero, then either there is no error, or it is a multiple of each of the divisors $d_{j-1 \ j}$, $d_{j \ j+1}$ (one-time error is assumed).

3. If $u_{j-1 \ j} \neq 0$, $u_{j \ j+1} \neq 0$, and all other values are $u_{jq} = 0$, then the error occurred modulo b_j , i.e. $\tilde{u}_j = u_j + \theta_j$ ($1 \leq \theta_j \leq b_j - 1$).

According to the proven Theorem 8, the condition (24) written in the general form is a necessary condition for correcting the error in the residual u_j :

$$(d_{jk} - 1)(d_{jq} - 1) \geq \delta(\theta_j), \quad (24)$$

$$\text{as well } \delta(\theta_j) = b_j - 1 - \left(N_{d_{jk}} + N_{d_{jq}} - N_{[d_{jk}, d_{jq}]} \right);$$

$N_{d_{jk}}$ is the number of possible divisors of the error θ_j by base b_j (that is, the number of possible divisors of the number $b_j - 1$) multiples of the value of d_{jk} ;

$N_{d_{jq}}$ is the number of possible divisors of error θ_j by base b_j multiples of d_{jq} ;

$K_{[d_{jk}, d_{jq}]}$ is the number of possible divisors of error θ_j by base b_j multiples of the LCM value of numbers d_{jk} and d_{jq} .

Condition (24) is sufficient if different possible values $\delta(\theta_j)$ of errors by base b_j ($j = \overline{1, g}$) correspond to different pairs of values u_{jk} and u_{jq} . Let's consider an example of a specific execution of an error correction operation in the SRC given by the bases $b_1 = 4$, $b_2 = 6$, $b_3 = 12$. And here the table of code words $L = P = LCM[4, 6, 12] = 12$ is presented in the form of a Table 5. Note that $d_{12} = (4, 6) = 2$, $d_{23} = (6, 12) = 6$, $d_{31} = (12, 4) = 4$, $\delta(\theta_1) = 2$ (see Table 6), $\delta(\theta_2) = 3$ (see Table 7), $\delta(\theta_3) = 8$ (see Table 8), as well:

$$\delta(\theta_1) = b_1 - 1 - \left(N_{d_{12}} + N_{d_{31}} - N_{[d_{12}, d_{31}]} \right),$$

$$\delta(\theta_2) = b_2 - 1 - \left(N_{d_{12}} + N_{d_{23}} - N_{[d_{12}, d_{23}]} \right),$$

$$\delta(\theta_3) = b_3 - 1 - \left(N_{d_{23}} + N_{d_{31}} - N_{[d_{23}, d_{31}]} \right).$$

Table 5. Decision table

u_{31}	$u_{12} = 1$
1	$\theta_1 = 1$
2	–
3	$\theta_3 = 3$

Table 6. Decision table

u_{23}	$u_{12} = 1$
1	$\theta_2 = 5$
2	–
3	$\theta_2 = 3$
4	–
5	$\theta_2 = 1$

Table 7. Decision table

u_{31}	u_{23}				
	1	2	3	4	5
1	$\theta_3 = 7$	–	$\theta_3 = 3$	–	$\theta_3 = 11$
2	–	$\theta_3 = 2$	–	$\theta_3 = 10$	–
3	$\theta_3 = 1$	–	$\theta_3 = 9$	–	$\theta_3 = 5$

Let it be necessary to determine the correctness of the number $U = (11 \parallel 100 \parallel 0111)$. The original number U is entered in the first and second input registers. The first adder of the first group determines the value of $\bar{u}_1 = b_1 - u_1 = 01$, the second: $\bar{u}_2 = b_2 - u_2 = 010$; and the third: $\bar{u}_3 = b_3 - u_3 = 0101$. The first adder modulo d_{jq} determines the value of $u_{12} = (u_1 + \bar{u}_2) \bmod_{12}$, the second – $u_{23} = (u_2 + \bar{u}_3) \bmod_{23}$, the third – $u_{31} = (u_3 + \bar{u}_1) \bmod_{31}$. Thus, from the outputs of the corresponding decoders, only the second commutator receives the values $u_{12} = 1$, $u_{23} = 3$, according to which (see Table 6) it determines the value of the inverted error modulo b_2 , i.e. $\theta_2 = 3$, which through the second decoder in the binary code is sent to the first input of the second adder, on the second input of which receives the value $\tilde{u}_2 = u_2 + \theta_2 = 100$. The adder of the second group determines the result of the operation:

$$(\theta_2 + u_2) \bmod b_2 = (b_2 - \theta_2 + u_2 + \theta_2) \bmod b_2 = 001.$$

The corrected number $U = (11 \parallel 001 \parallel 0111)$ is received at the input of the device (see Table 4). Thus, error correction algorithms in SRC with mutually pairwise non-prime bases make it relatively easy to implement the procedure for detecting and correcting one-time errors. The considered scheme for detection and correction of single errors allows to localize the erroneous base and correct the error in one residue in just five conditional time cycles for any number of SRC bases. The main advantages of L -codes in the SRC are the simplicity of the procedure for detecting the location of the error and its localization. In terms of the simplicity of decoding schemes, L -codes have no analogues, both in the PNS and in the SRC. Codes in the SRC with mutually pairwise non-prime bases can be used in the construction of decoders to create high-reliability and fast-acting IPS of the ARP, where the criterion of redundancy of presentation of word codes is not of decisive importance.

CONCLUSION

As a result of the large-scale war launched by the Russian Federation against Ukraine, the issues of strengthening all types of security to ensure the integrity and sovereignty of the country became topical. Information security is a priority direction. The rapid spread of the latest technologies in the information field, artificial intelligence technologies, the development of robotics, changes in the forms and methods of conducting armed conflict require new approaches to military-technical support. The need to modernize military equipment based on the security of information and communication systems is indisputable.

Modern coding theory has at its disposal a large arsenal of methods and means for increasing the informational reliability of the IPS. Wide implementation of information reservation methods, which would allow control of errors in processing systems, is facilitated by the use of codes in the SRC.

In general, information reservation involves the use of redundancy of information coming to the object. It is implemented by introducing redundant codes and symbols during the transmission, processing and display of information (for example, additional units of information that allow detecting and eliminating errors in the transmission of information: correction codes, checksums, parity checks, etc.).

The use of information reservation methods allows us to take into account the fact that the ARP itself, in the end, is not interested in either the size of the error or its location. The very essence is based on probabilistic hypotheses about the multiplicity of errors. The main indicator is only information that is correct according to some criterion for further use. This feature should be laid down even during the design of the IPS of the ARP.

The code that would be able to control the errors that occur in the IPS of the ARP, primarily requires arithmeticity. Arithmeticity of an error-controlling code is understood as its property, which consists in the fact that when any arithmetic operation is performed on two correct (not distorted) code words (numbers), the result is also a correct code word. That is, the arithmeticity of the code makes it possible to control errors when performing arithmetic operations. At the same time, it is desirable that in the process of calculation, errors do not move from digit to digit, so that the negative phenomenon of faults connections does not arise. Codes satisfying the above requirements are known. One of the representatives of this class of codes is the codes in the SRC. In the SRC, operations on residues are carried out according to the rules of modular arithmetic, so many points of a given space of residues will satisfy all axioms of addition and multiplication, i.e., the code in the residues is an arithmeticity code. The advantage of such a code is that it can be used both to check the correctness of arithmetic operations and to increase interference immunity.

The versatility of the SRC codes is explained not only by its high correcting abilities, arithmeticity and the ability to deal with error packets, but also by its adaptability to flexible changes in correcting properties, without changing the coding method. SRC opens up the possibility of using a single failure-resistant code to combat errors that occur during data transmission and processing in the IPS of the ARP.

Let's note if some chain of arithmetic operations is performed by the program, the true result of which, in the absence of errors during the calculation, should be the correct

number, and let there be a failure in the numbers by some base b_j at one stage of the calculation process. Then the final result of the circuit can contain an error only by base b_j . In other words, in the process of calculation, the errors that arises keep its places and do not move to the bases, which are not disturbed by the primary error.

The main requirements for the IPS of the ARP are high reliability and survivability. Since it is fundamentally impossible to create absolutely reliable system components, another, new direction has emerged – fault-tolerant computing systems, that is, systems that are able to continue functioning in the event of various failures and failures of a part of the equipment.

There are two directions for improving the reliability of computer systems: preventing faults and creating fault-tolerant systems.

When using the first direction, it tries to eliminate all possible sources of failure by constructing a system from highly reliable components. However, in this case, as the intensity of element failures approaches the threshold values determined by physical parameters or technology, the cost of the system increases sharply. In addition, since at the first failure or denial, the normal functioning of the system ceases, and its operation requires permanent personnel, which leads to an increase in the cost of the system.

When using the second direction, the probability of failure of components does not decrease, but additional requirements are imposed on the system: it must work without errors when individual components fail. These additional requirements and, therefore, fault-tolerant operation of the system is ensured by the introduction of various forms of redundancy: hardware, software and time.

Redundancy can be used to improve other important characteristics of computational structures. Computational structures implemented on the basis of non-positional numeral systems, which make it possible to eliminate transfer time when performing arithmetic operations, have wide prospects. The latter in many cases makes it possible to increase reliability, survivability and speed at the same time with moderate expenditure of hardware. One of such numeral systems is the SRC.

The generalized algorithm of functioning of any fault-tolerant system is reduced to the following standard procedures:

- detection of failure in the system;
- diagnosing the failed device;
- assessment of the damage caused by the failure;
- elimination of the failed device and restoration of lost information.

At the same time, the means of ensuring fault tolerance of computer systems operating in the PNS have a number of significant shortcomings. The main ones are:

- significant hardware and software costs, necessary for the implementation of a fault-tolerant special processor;
- the use of structural reservation, both at the level of a separate computing module and at the level of the entire parallel system, complicates the computing complex and increases its energy consumption;
- the complexity of implementing search procedures and error localization in the calculation process;
- the difficulty of writing and implementing a self-test program;
- significant time costs for reconfiguration of the structure;

- the need to restart the program after restoring the functional structural design of the IPS, which is unacceptable when performing tasks on a real-time scale.

At the same time, the structure of non-positional IPS approaches a high degree of homogeneity, which makes it possible to significantly improve such a parameter as survivability.

In the same way, the use of the SRC ensures independent and parallel processing of each digit of the number. Taking into account the low bit rate of the processed operands, IPS in the SRC can be performed in the form of a set of tables for the implementation of a number of basic modular operations.

Excessive coding in the SRC ensures the survivability of the equipment even in catastrophic situations, when the flow of faults is very large. Such a system will produce a result with less accuracy or with a slightly slower, but quite sufficient, speed of operation for the high-quality functioning of the equipment.

It should be noted that the SRC with two control bases allows you to fully preserve the performance of the special processor in case of failures of any two elements. And when the third and even fourth failure occurs, it can still execute the program with some reduction in accuracy and speed of calculations.

This property is one of the factors on which the development of a structure of fault-tolerant non-positional IPS with gradual degradation without a noticeable increase in hardware costs, i.e. reservation, is based, and ensures the creation of computing systems that allow for the possibility of continued operation in the event of the failure of part of the elements of the structure.

The combination of requirements for high reliability and fast data processing allows creating a unique structure of a non-positional neurocomputer thanks to the modular organization of information processing, transmission and storage.

Thus, the concept of the development of high-speed computer components of the computing system for processing integer data in the SRC consists in the development and application of methods and means of operational control, diagnosis and correction of data errors.

The use of the developed methods of operational control, diagnostics and correction of data errors will allow eliminating the conflict situation between the existing possibility of significantly increasing the speed of performing integer arithmetic operations in the SRC and the low efficiency of the existing systems and means of control, diagnostics and correction of calculation results in the SRC. This, in turn, will resolve the contradiction between the high speed of implementation of integer arithmetic operations and the low efficiency of control, diagnosis and correction of data in the SRC.

Thus, from the above material, it is obvious that the existing methods of control, diagnosis and correction (detection and correction) of data errors, which are presented in the SRC, do not always satisfy the growing requirements for its efficiency. The complexity of the technical implementation and the significant time of data control, diagnosis and correction deprives one of the advantages of the SRC – ultra-fast implementation of the process of processing integer data. The above-mentioned shortcoming of the processes of control, diagnosis and correction data of the IPS operating in the SRC, on the one hand, and positive preliminary research results devoted to the possibility of increasing the efficiency

of these processes, on the other hand, have not been eliminated, and determined the goal, the scientific and practical task of this monograph.

In order to determine the possibility of creating effective systems and means of operational control, diagnostics and correction of data in the SRC, the principles of building non-positional code structures are formulated in the monograph. On the basis of the formulated principles of construction of non-positional code structures, studies of the influence of the SRC properties on the structure and process of functioning of components of the IPS of the ARP were carried out. The results of the study formed the basis of the analysis of the corrective possibilities of the codes in the SRC. The main provisions and conclusions of the theory of failure-resistant data coding in the SRC are presented. On the basis of the provisions of the theory of failure-resistant data coding, studies of corrective properties and possibilities of non-positional code structures were carried out with different methods of introducing information redundancy, i.e. with different number and size of additional control bases. This made it possible to create a procedure for varying the possible corrective capabilities of the failure-resistant code in the SRC during the computational process.

The main attention is focused on the given theoretical basis of correction of data errors in the SRC. Using the main theoretical provisions of the correction of non-positional code structures, the monograph presents a method of detecting and correcting errors in the SRC based on linear L -codes. It is shown that the use of L -codes with mutually non-prime bases allows expanding the class of errors that is corrected. This significantly expands the corrective capabilities of L -codes in the SRC. The developed error correction algorithms in the SRC make it relatively simple to implement the procedure for detecting and correcting single errors. The developed method of detecting and correcting errors based on the application of linear L -codes differs from the widely used R -codes in the SRC by the simplicity of the decoding operation of non-positional code structures (the technical simplicity of the decoding device), and the high speed of the operation of detecting and correcting errors in the code word. The main advantages of L -codes in the SRC are the simplicity of the procedure for detecting the location of the error and its localization. Also, in terms of the simplicity of decoding schemes, L -codes have no analogues, both in the PNS and in the SRC. The use of the proposed method of detecting and correcting data errors increases the overall efficiency and feasibility of using non-positional code structures in the SRC in modern IPS.

REFERENCES

1. Onyshchenko, S., Yanko, A., Hlushko, A., & Maslii, O. (2023). Economic cybersecurity of business in Ukraine: strategic directions and implementation mechanism. *Economic and cyber security* (c. 30–58). Privat Company Technology Center. URL: <https://doi.org/10.15587/978-617-7319-98-5.ch2>
2. Krasnobayev, V., Yanko, A., & Hlushko, A. (2023). Information Security of the National Economy Based on an Effective Data Control Method. *Journal of International Commerce, Economics and Policy*. URL: <https://doi.org/10.1142/s1793993323500217>
3. Victor, K., Yanko, A., Hlushko, A., Kruk, O., Kruk, O., & Gakh, V. (2023). Cyberspace protection system based on the data comparison method. *Y Economic and cyber security* (c. 3–29). Privat Company Technology Center. URL: <https://doi.org/10.15587/978-617-7319-98-5.ch1>
4. Krasnobayev, V., Kuznetsov, A., Yanko, A., Koshman, S., Zamula, A., & Kuznetsova, T. (2019). *Data processing in the system of residual classes*. ASC Academic Publishing.
5. Chappell, J., Demery, Z. P., Arriola-Rios, V., & Sloman, A. (2012). How to build an information gathering and processing system: Lessons from naturally and artificially intelligent systems. *Behavioural Processes*, 89(2), 179–186. URL: <https://doi.org/10.1016/j.beproc.2011.10.001>
6. Silva, A. C. d. P., & Loureiro, G. (2022). Simultaneous and collaborative development of satellites and Information Systems to support its lifecycle processes. *Information Systems*, 102125. URL: <https://doi.org/10.1016/j.is.2022.102125>
7. An, Y., Wong, J., & Ling, S. H. (2024). Development of real-time brain-computer interface control system for robot. *Applied Soft Computing*, 159, 111648. <https://doi.org/10.1016/j.asoc.2024.111648>
8. Jiang, S., Qi, P., Han, L., Liu, L., Li, Y., Huang, Z., Liu, Y., & He, X. (2024). Navigation system for orchard spraying robot based on 3D LiDAR SLAM with NDT_ICP point cloud registration. *Computers and Electronics in Agriculture*, 220, 108870. <https://doi.org/10.1016/j.compag.2024.108870>
9. Topalov, A. (2023). Analiz mikroelektronnykh tsyfrovyykh prystroyiv zboru, obrobky i peredachi danykh v robototekhnichnykh systemakh [*Analysis of microelectronic digital devices for data collection, processing and transmission in robotic systems*]. *Materialy vseukrayins'koyi naukovo-praktychnoyi konferentsiyi molodykh uchenykh i studentiv «Informatsiyni tekhnolohiyi v osviti, tekhnitsi ta promyslovosti» – Materials of the All-Ukrainian scientific and practical conference of young scientists and students "Information technologies in education, technology and industry"*. [in Ukrainian]
10. Pastor, E., Lopez, J., & Royo, P. (2006). A Hardware/Software Architecture for UAV Payload and Mission Control. *Y 2006 ieee/aiaa 25TH Digital Avionics Systems Conference*. IEEE. <https://doi.org/10.1109/dasc.2006.313738>

11. Luhovs'kyi H., & Vorotnikov V. (2021). Systema kontrolyu informatsiynykh potokiv u komp'yuterniy merezhi student's'koho hurtozhytku. [*Information flow control system in the computer network of the student dormitory*]. *Informatsiyni systemy ta komp'yuterno-intehrovani tekhnolohiyi: ideyi, problemy, rishennya – 2021* (c. 40–42). [in Ukrainian]
12. Shahlaei, M., & Hashemi, S. M. (2024). A risk-aware and recommender distributed intrusion detection system for home robots. *Journal of Information Security and Applications*, 83, 103777. <https://doi.org/10.1016/j.jisa.2024.103777>
13. Sato, Y., Kakuto, T., Tanaka, T., Shimano, H., Morohashi, Y., Hatakeyama, T., Nakajima, J., & Ishiyama, M. (2024). Development of a radioactive substance detection system integrating a Compton camera and a LiDAR camera with a hexapod robot. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 169300. <https://doi.org/10.1016/j.nima.2024.169300>
14. Değirmenci, E., Sabri Kırca, Y., Özçelik, İ., & Yazıcı, A. (2023). ROSIDS23: Network Intrusion Detection Dataset for Robot Operating System. *Data in Brief*, 109739. <https://doi.org/10.1016/j.dib.2023.109739>
15. Tian, Y., Mai, Z., Zeng, Z., Cai, Y., Yang, J., Zhao, B., Zhu, X., & Qi, L. (2023). Design and experiment of an integrated navigation system for a paddy field scouting robot. *Computers and Electronics in Agriculture*, 214, 108336. <https://doi.org/10.1016/j.compag.2023.108336>
16. Krainov, O., & Hrozovskyi, R. (2019). Metodyka otsinky operatyvnosti obrobky informatsiyi systemoyu informatsiyno-analitychnoho zabezpechennya orhanu viys'kovoho upravlinnya [*Methodology for evaluating the efficiency of information processing by the information and analytical support system of the military management body*]. *Suchasni informatsiyni tekhnolohiyi u sferi bezpeky ta oborony*, 34(1), 147–150. <https://doi.org/10.33099/2311-7249/2019-34-1-147-150> [in Ukrainian]
17. Khomyuk, V. V. (2002). Metody poperedn'oyi obrobky informatsiyi v protsesi rozpoznavannya obraziv [*Methods of preprocessing information in the process of pattern recognition*]. *Visnyk Sums'koho derzhavnoho universytetu*. Retrieved from: <https://sal0.li/a5e86BC> [in Ukrainian]
18. Fonseca, J. V., Oliveira, R. C. L., Abreu, J. A. P., Ferreira, E., & Machado, M. (2013). Kalman Filter Embedded in FPGA to Improve Tracking Performance in Ballistic Rockets. *Y 2013 UKSim 15th International Conference on Computer Modelling and Simulation (UKSim 2013)*. IEEE. <https://doi.org/10.1109/uksim.2013.149>
19. Histoshi Nohmi, Shiro Kato, Nobuyasu Ito, Takenori Yanase Hiromu Kashihara, Kenji Naito, & Shinichi Hanaki. *Digital Processing of Space-borne Synthetic Aperture Radar Data*. Asian Association on Remote Sensing | ACRS | AARS. <https://a-a-r-s.org/proceeding/ACRS1980/Papers/DCA80-1.html>
20. Radar and Sensors. *FPGA for Military Applications – Intel® FPGA*. URL: <https://www.intel.com/content/www/us/en/government/products/programmable/applications.html>

21. Zhuravel', S., Dumych, S., & Shpur, O. (2021). Doslidzhennya metodiv zboru ta obrobky danykh v rozpodilennykh informatsiynykh systemakh [*Study of methods of data collection and processing in distributed information systems*]. *Information and communication technologies, electronic engineering*, 1(1), 20–38. URL: <https://doi.org/10.23939/ict2021.01.020> [in Ukrainian]
22. Pratsiovytyi, M., Bondarenko, O., Ratushniak, S., & Franchuk, K. (2022). $\bar{Q}$ -representation of Real Numbers as a Generalization of Cantor Numeral Systems. *Mohyla Mathematical Journal*, 5, 9–18. URL: <https://doi.org/10.18523/2617-7080520229-18>
23. Borysenko, O. A. (2007). Chyslo i systemy chyslennya v elektronnykh chyslovykh systemakh [*Number and counting systems in electronic numerical systems*]. *Visnyk SumDU. Seriya "Tekhnichni nauky"*, (4), 71–76. [in Ukrainian]
24. Titov, S., Titova, O., & Chorna, O. (2022). Opys neskorotnykh naboriv oznak v pryblyzhnykh mnozhynakh z vykorystannyam system chyslennya [*Description of irreducible sets of features in approximate sets using number systems*]. *Zbirnyk naukovykh prats' Kharkivs'koho natsional'noho universytetu Povitryanykh Syl*, (1(71)), 106–110. [in Ukrainian]
25. Bondarenko, O. I., Vasilenko, N. M., & Prats'ovytyy, M. V. (2019). Kantorivs'ka divykovy-fibonachchiyevasystema chyslennya u zadachakh teoriyifunktsiy [*Cantor's binary-Fibonacci calculation system in function theory problems*]. *Zbirnyk prats' Intu matematyky NAN Ukrayiny*, 16(3), 174–186. [in Ukrainian]
26. Azarov, O. D., Reshetnik, O. O., & Bohomolov, S. V. (2008). Systemy chyslennya z vahovoyu nadlyshkovistyuu dlya shvydkodiyuchykh ATSP poslidoynoho nablyzhennya i TSAP, shcho samokalibruyut'sya [*Counting systems with weight redundancy for high-speed sequential approximation ADCs and self-calibrating DACs*]. *Naukovi pratsi VNTU*, (3), 1–8. [in Ukrainian]
27. Kulyk, I. A., & Shevchenko, M. S. (2020). Rozrobka informatsiyno-keruyuchykh system na osnovi divykovoyi binomial'noyi systemy chyslennya [*Development of information and control systems based on the binary binomial number system*]. *Systemy obrobky informatsiyi*, (2(161)), 78–85. <https://doi.org/10.30748/soi.2020.161.09> [in Ukrainian]
28. Krasnobayev, V., Koshman, S., Kurchanov, V., & Zinevich, D. (2019). Osnovni vlastyivosti nepozytsiynoyi systemy chyslennya u klasi lyshkiv i yikh vplyv na strukturu ta pryntsypy realizatsiyi aryfmetychnykh operatsiy komp'yuternoyi systemy [*The main properties of the non-positional counting system in the class of remainders and their influence on the structure and principles of implementation of arithmetic operations of the computer system*]. *Systemy upravlinnya, navihatsiyi ta zv'yazku. Zbirnyk naukovykh prats'*, 2(54), 114–118. <https://doi.org/10.26906/sunz.2019.2.114> [in Ukrainian]
29. Krutskevych, O. Metod ta alhorytm mnozhennya u dvovymirniy systemi chyslennya matrychnoho Rademakhera [*The method and algorithm of multiplication in the two-dimensional Rademacher matrix calculation system*]. 148–151. Retrieved

from: <https://science.lpnu.ua/sites/default/files/journal-paper/2017/nov/7083/25-148-151.pdf> [in Ukrainian]

30. Borysenko, O., Kalashnikov, V., & Kalashnykova, N. (2016). Opys ta zastosuvannya binomial'nykh system chyslennya [*Description and application of binomial counting systems*]. *Komp'yuterni nauky ta kiberbezpeka*, (2), 13-21. <https://periodicals.karazin.ua/cscs/article/view/6208> [in Ukrainian]
31. Mel'nyk, O. H. (2011). Skhemotekhnichni osnovy realizatsiyi systemy zalyshkovykh klasiv v dviykovo-chetvirkoviy systemi chyslennya [*Schematic and technical foundations of the implementation of the system of residual classes in the binary-quadruple number system*]. *Systemy obrobky informatsiyi*, (8), 93–95. [in Ukrainian]
32. Yatskiv, V. V. (2015). Kontrol' vykonannya aryfmetychnykh operatsiy na osnovi modulyarnykh kodiv [*Control of arithmetic operations based on modular codes*]. *Vymiryuval'na ta obchyslyuval'na tekhnika v tekhnolohichnykh protsesakh*, (4), 135–138. [in Ukrainian]
33. Yatskiv, Vasyl. (2014). The modular operations methods and its implementation on cpld. *Herald of Khmelnytskyi national university*. 219. 218-224.
34. Prasad, K., & Sundar Rajan, B. *A Matroidal Framework for Network-Error Correcting Codes*. arXiv.org. <https://arxiv.org/abs/1201.6459>
35. Krasnobayev, V. A., Yanko, A. S., Kurchanov, V. N., & Koshman, S. A. (2016). The analysis of the tasks and algorithms of data integer processing in the residual classes system. *Naukovo-tekhnichnyy zhurnal «Radioelektronni i komp'yuterni systemy»*, (1(75)), 19–28.
36. Krasnobayev, V., Yanko, A., & Kovalchuk, D. (2023). Control, Diagnostics and Error Correction in the Modular Number System. *Computer Modeling and Intelligent Systems*, 3392, 199–213. <https://doi.org/10.32782/cmis/3392-17>
37. Yanko, A., Krasnobayev, V., & Martynenko, A. (2023). Influence of the number system in residual classes on the fault tolerance of the computer system. *Radioelectronic and Computer Systems*, (3), 159–172. <https://doi.org/10.32620/reks.2023.3.13>
38. Yanko, A. S., Krasnobayev, V. A., Nikolsky, S. B., & Kruk, O. O. (2024). Method for determining the bit grid overflow of a computer system operating in the system of residual classes. *Radio Electronics, Computer Science, Control*, (1), 228. <https://doi.org/10.15588/1607-3274-2024-1-21>
39. Krasnobayev, V., Koshman, S., Yanko, A., & Martynenko, A. (2018). Method of Error Control of the Information Presented in the Modular Number System. *Y 2018 International Scientific-Practical Conference Problems of Infocommunications. Science and Technology (PIC S&T)*. IEEE. <https://doi.org/10.1109/infocommst.2018.8632049>
40. Onyshchenko, S., Yanko, A., & Hlushko, A. (2023). Improving the efficiency of diagnosing errors in computer devices for processing economic data functioning in the class of residuals. *Eastern-European Journal of Enterprise Technologies*, 5(4 (125)), 63–73. <https://doi.org/10.15587/1729-4061.2023.289185>

41. Ponochovnyi, Y., Bulba, E., Yanko, A., & Hozbenko, E. (2018). Influence of diagnostics errors on safety: Indicators and requirements. *Y 2018 IEEE 9th International Conference on Dependable Systems, Services and Technologies (DESSERT)*. IEEE. <https://doi.org/10.1109/dessert.2018.8409098>
42. Onyshchenko, S., Yanko, A., Hlushko, A., & Sivitska, S. (2021). Increasing Information Protection in the Information Security Management System of the Enterprise. *Y Lecture Notes in Civil Engineering* (c. 725–738). Springer International Publishing. https://doi.org/10.1007/978-3-030-85043-2_67
43. Krasnobayev, V., Kuznetsov, A., Yanko, A., & Kuznetsova, K. (2019). Correction Codes in the System of Residual Classes. *Y 2019 IEEE International Scientific-Practical Conference Problems of Infocommunications, Science and Technology (PIC S&T)*. IEEE. URL: <https://doi.org/10.1109/picst47496.2019.9061253>
44. Krasnobayev, V., Kuznetsov, A., Yanko, A., & Kuznetsova, T. (2020). The analysis of the methods of data diagnostic in a residue number system. *3rd International Workshop on Computer Modeling and Intelligent Systems (CMIS-2020)*, 2608, 594–609. URL: <https://doi.org/10.32782/cmisi/2608-46>
45. Krasnobayev, V., Kuznetsov, A., Yanko, A., & Kuznetsova, K. (2020a). The data errors control in the modular number system based on the nullification procedure. *3rd International Workshop on Computer Modeling and Intelligent Systems (CMIS-2020)*, 2608, 580–593. URL: <https://doi.org/10.32782/cmisi/2608-45>
46. Yanko, A., Krasnobayev, V., & Martynenko, A. (2019). The implementation of L-codes in the system of residual classes. *Fundamental'nye I Prikladnye Issledovaniâ V Praktikh Veduših Naučnyh Škol*, 34(4), 55–65. URL: <https://doi.org/10.33531/farplss.2019.4.8>

**DATA ERROR CORRECTION METHOD FOR INCREASING THE
INFORMATION PROTECTION OF AN AUTOMATED ROBOTIC
PLATFORM**

Monograph

Alina Yanko, Oleksandr Laktionov, Nazar Pedchenko, Stanislav Bilko

Data Error Correction Method for Increasing the Information Protection of an Automated Robotic Platform: A monograph / A., Yanko, O., Laktionov, N., Pedchenko, S., Bilko. – Warsaw: E-SCIENCE SPACE, 2024 – 62 p.

ISBN 978-83-961636-5-3

DOI 10.54658/ESS.monograph.2024.pp.1-62

UDC 681.5.09 (004.056.2/.5)

State No. registration number 00124U000621

Authors responsible for the content or accuracy of the information

Layout 60x84/8. Printed sheets 37,65. Run 1000 copies.

Order № 01/01-2024

PUBLISHED AND PRINTED BY THE E-SCIENCE SPACE SPÓŁKA Z

OGRANICZONĄ ODPOWIEDZIALNOŚCIĄ

KRS 870645, SZCZĘSNA 26, 02-454 Warszawa, Polska

Identyfikator wydawcy w e-ISBN 40907

Kontakt tel. +48739692146

<https://e-science.space/en/publications/>

